HEWLETT hp PACKARD

SERVICE MANUAL

7970B/E

DIGITAL MAGNETIC TAPE UNITS

Manual Part No. 07970-90887
Microfiche Part No. 07970-90894

Serial Numbers Prefixed:
7970B--1107 thru 1536
7970E--1127 thru 1542

HEWLETT-PACKARD COMPANY
15 N. PHILLIPPI ST., BOISE, IDAHO, U.S.A.

Title Page

SECTION I. GENERAL INFORMATION

SECTION II. INSTALLATION

TABLE OF CONTENTS (CONTINUED)

Title Page

SECTION IV. THEORY OF OPERATION (CONTINUED)

SECTION V. MAINTENANCE AND TROUBLESHOOTING

TABLE OF CONTENTS (CONTINUED)

Title Page

SECTION V. MAINTENANCE AND TROUBLESHOOTING (CONTINUED)

Title Page

SECTION V. MAINTENANCE AND TROUBLESHOOTING (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

Title Page

SECTION V. MAINTENANCE AND TROUBLESHOOTING (CONTINUED)

FIGURES

Figure Page

FIGURES (CONTINUED)

TABLES

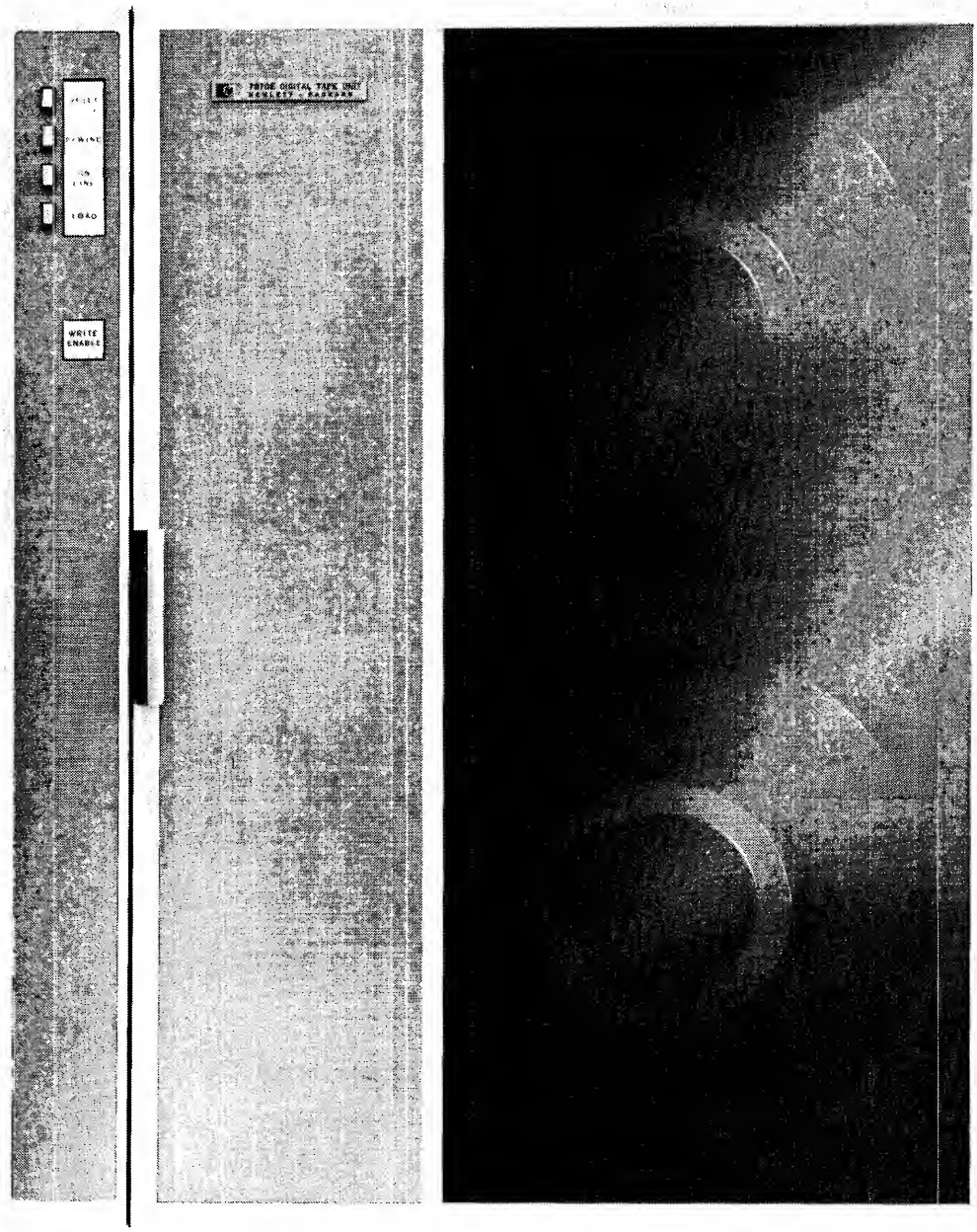


Figure 1-1. HP 7970B/E Digital Magnetic Tape Unit

GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION.

This manual provides operating, theory of operation and servicing information for standard configurations of the 7970B/7970E Digital Magnetic Tape Units (figure 1-1). Special product configurations are described by supplements, which accompany this manual.

This manual is divided into the four following sections:

Section I contains general and operator information.

Section II contains installation information.

Section III contains theory of operation.

Section IV contains maintenance information.

The parts information and schematics are covered in a separate manual. (Part No. 07970-90886). The schematics will be referred to during the explanations in this text.

1-2. DESCRIPTION.

The HP 7970B and 7970E Digital Magnetic Tape Units and options provide Non Return to Zero Inverted (NRZI) format in seven or nine track operation (7970B) and Phase Encoded (PE) or PE/NRZI formats in seven or nine track operation (7970E). Various configurations include read-only and read/write circuits, depending on the options selected.

The tape unit is designed as a peripheral unit for small computer systems and miscellaneous applications. (i.e., plotting table control, key edit systems, tape to microfilm, library programs, etc.). The read/write functions and the on-line tape control functions are computer programmable.

NOTE: For the following discussions refer to figure 1-2 and 1-3 to locate the assemblies discussed.

The assemblies and subassemblies which comprise the standard tape units can be grouped into six categories; control assemblies, transport assemblies, magnetic tape head assembly, read assemblies, write assemblies, and power distribution assemblies.

1-3. IDENTIFICATION.

Each tape unit has a model plate and a serial number plate. It is attached to the transformer assembly or just in front of the transformer assembly in left side of tape drive housing. The model plate indicates the tape speed of the unit and the model configuration. Table 1-1 lists the standard configuration option number and table 1-2 lists factory installed elective options which will appear on the model plate. When special product considerations exist (indicated by alphanumeric option numbers) the information is provided by special modification notices, supplemental

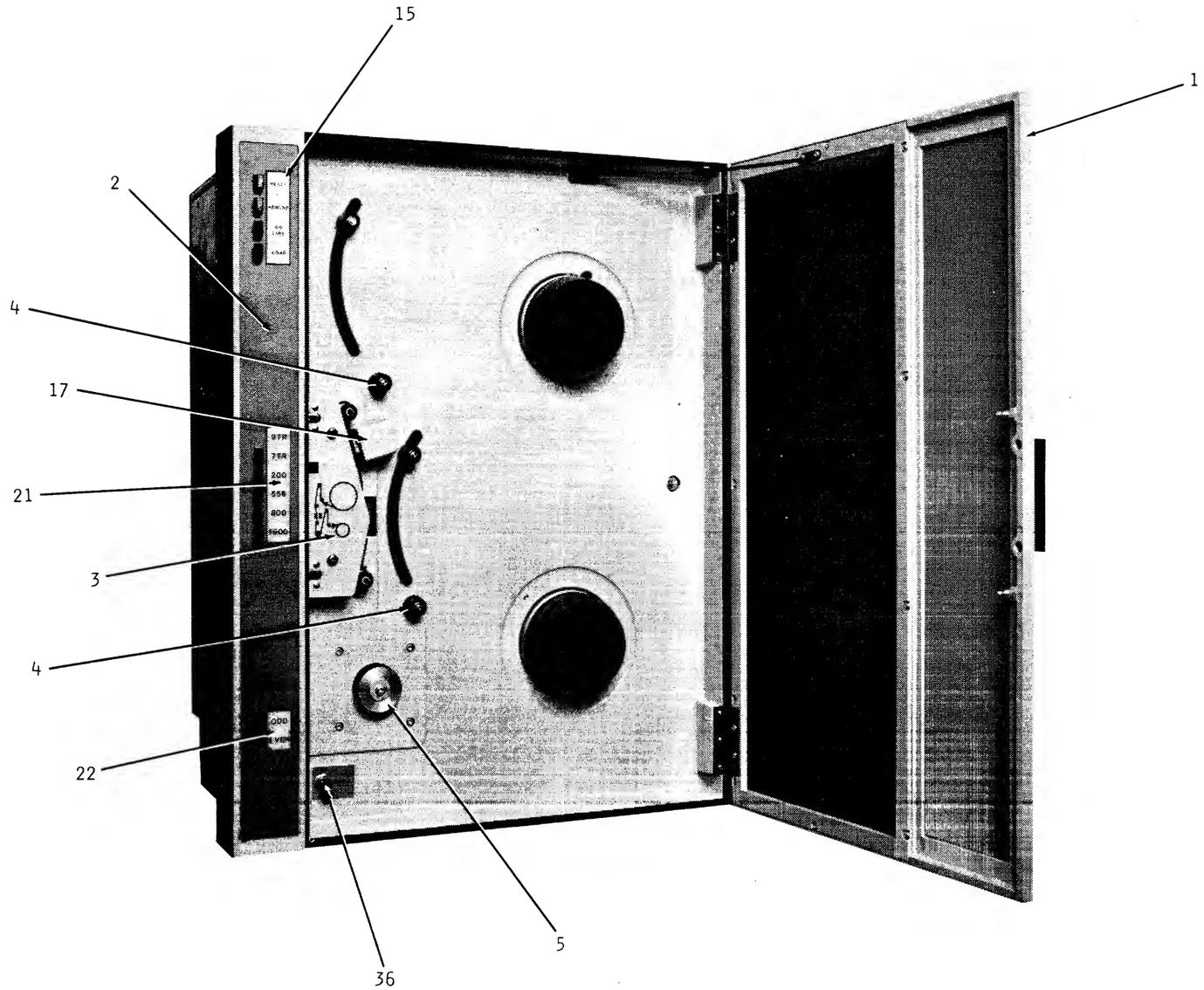
TABLE 1-1 7970B/7970E MAGNETIC TAPE UNIT CONFIGURATION GUIDE

Model-Option	Density											
	200	556	800	1600	Master	Slave	7-tr	9-tr	NRZI	PE	RO	RAW
7970B-127			X		NA	NA		X	X			X
7970B-136	X	X	X		NA	NA	X		X			X
7970E-150				X		X		X		X		X
7970E-151				X	X			X		X		X
7970E-152				X		X		X		X	X	
7970E-153				X	X			X		X	X	
7970E-162			X	X		X		X	X	X	X	
7970E-163			X	X	X			X	X	X	X	
7970E-164	X	X	X	X		X	X	X	X	X	X	
7970E-165	X	X	X	X	X		X	X	X	X	X	

TABLE 1-2 7970B/7970E ELECTIVE OPTIONS

NOTES: (1) RO-Read Only
(2) RAW-Read After Write
(3) All units are 45 ips speed unless speed option selected below
(4) All units have HP logo unless deleted by option below
(5) Power cord supplied for 115V (U.S., Canada, Japan, Mexico, Phillipines, Taiwan), unless option selected below

Elective Options:
001- 37.5 ips
002- 25.0 ips
003- 22.5 ips (7970E only)
004- Extender P.C. boards 7970B
004- Extender P.C. boards 7970E
005- Three I-O connectors
007- Unit select switch (not available with Option 020)
011- Delete HP logo
020- Parity select switch (7970E-164 or 165 only, not available with option 007)
021- Dual speed (7970E-162 through 165 only), lower speed is ½ indicated speed
048- DC Power
715- Service documentation
900- Substitutes power cord for use with 230V in Great Britain, Cyprus, Nigeria, Rhodesia, Singapore, South Africa, and India
901- Substitutes power cord for use with 230V in Australia, and New Zealand
902- Substitutes power cord for use with 230V in Europe, and Middle East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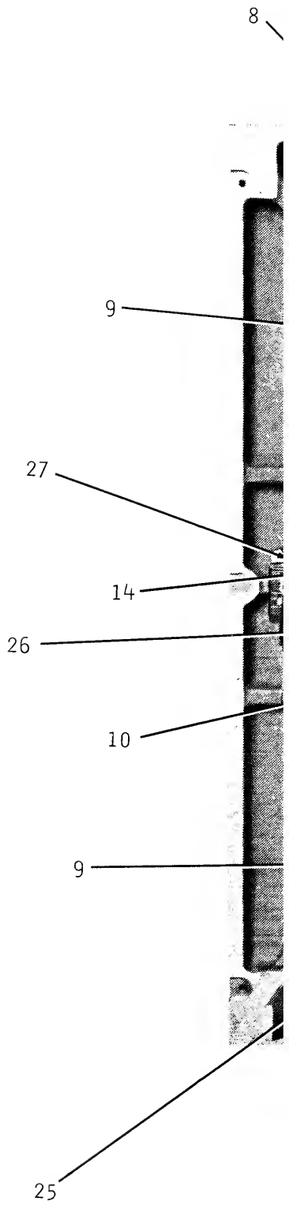
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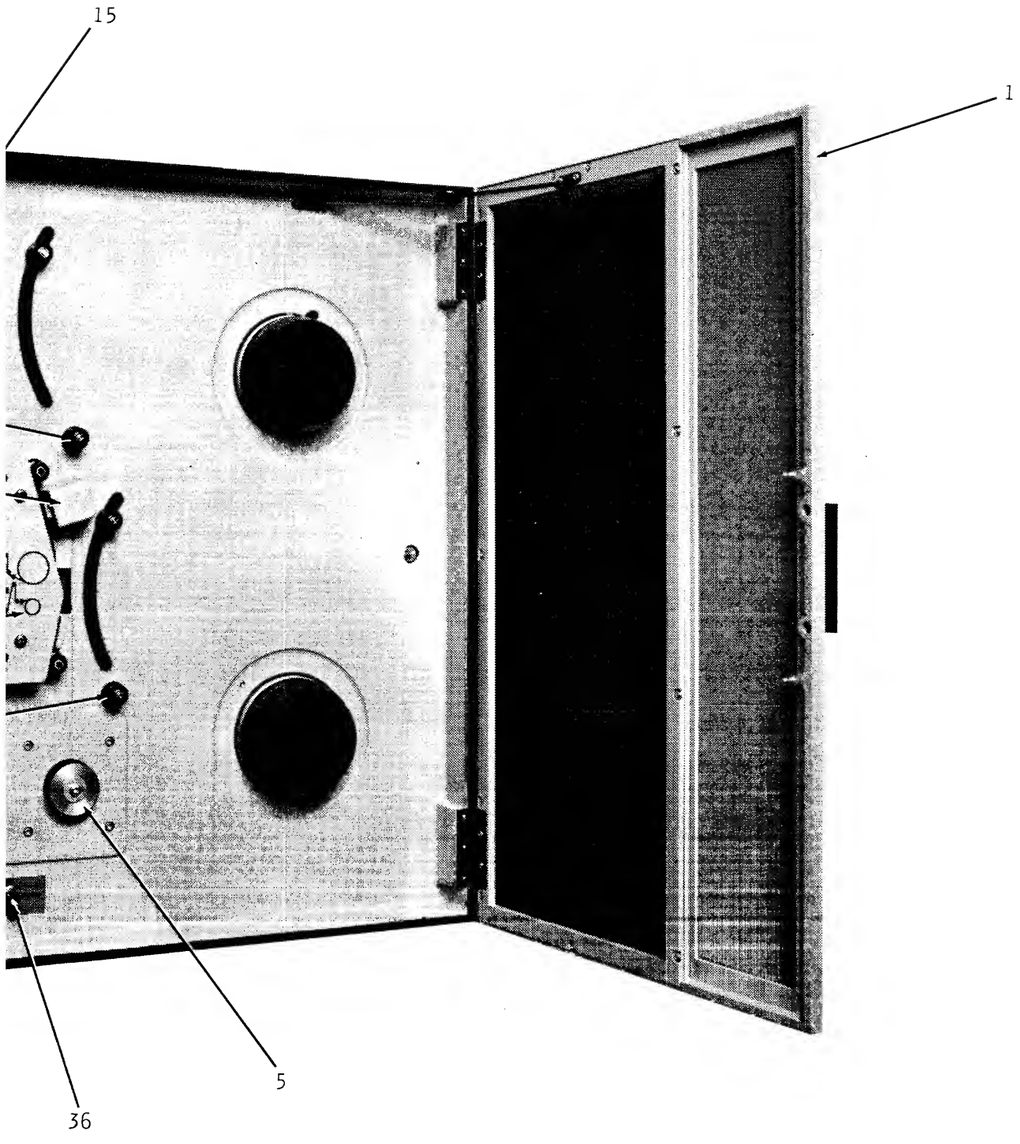


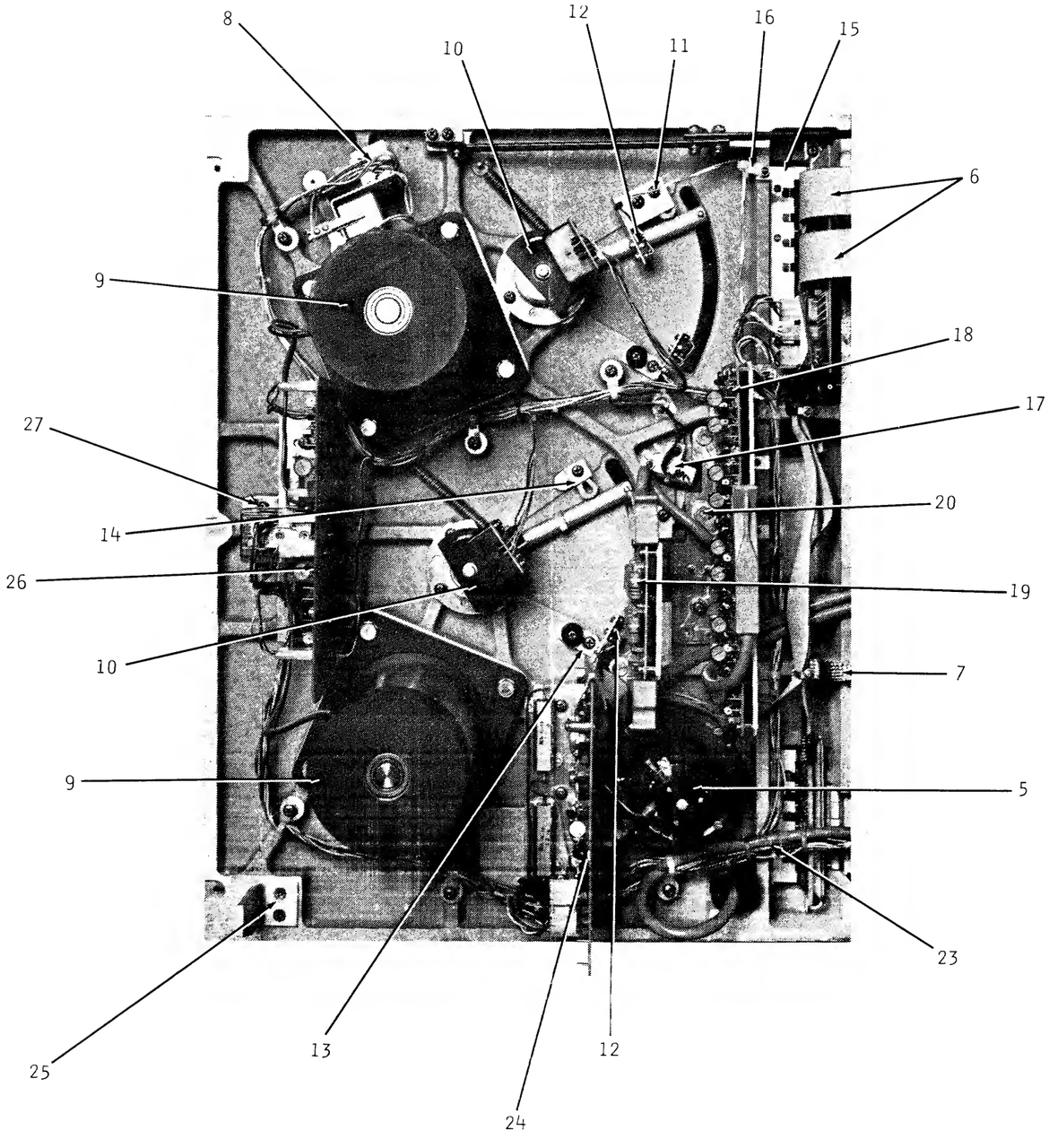


Figure 1-2. Open View Identification

Table 1-3. Tape Units Selected Component and Assembly Location

REF. DES.	DESCRIPTION	REF. DES.	DESCRIPTION
	7970B/E DIGITAL MAGNETIC TAPE UNIT		7970B/E DIGITAL MAGNETIC TAPE UNIT
1	Cover Door Assembly	22	PARITY SELECT SWITCH ASSEMBLY
2	PANEL, Switch Cover	23	TRANSPORT HARNESS ASSEMBLY
3	COVER, Head Assembly	24	CAPSTAN SERVO ASSEMBLY
4	TAPE ROLLER AND BEARING ASSEMBLY	25	GUIDE, Lifter
5	CAPSTAN MOTOR ASSEMBLY (MG 1)	26	REEL SERVO ASSEMBLY
6	RIBBON CABLE ASSEMBLY	27	PANEL FASTENER
7	GROUND STRAP	28 or	WRITE ASSEMBLY
8	WRITE ENABLE ASSEMBLY	28	NRZI READ ASSEMBLY (7970E Multiformat unit only)
9	REEL MOTOR ASSEMBLY (B1/B2)	29 or	RIBBON CABLE ASSEMBLY (read only drives)
10	TENSION ARM ASSEMBLY	29 or	RIBBON CABLE ASSEMBLY (read/write drives)
11	BRACKET, Limit Switch, Upper	29 or	RIBBON CABLE ASSEMBLY (PE read/write drives)
12	SWITCH, Limit Sensing, SPDT (W2S1, W2S2, W2S3)	29	RIBBON CABLE ASSEMBLY (PE read only drives)
13	BRACKET, Limit Switch, lower	30	READ ASSEMBLY
14	BUMPER, Rubber	31	POWER REGULATOR ASSEMBLY
15	CONTROL SWITCH ASSEMBLY	32	POWER DISTRIBUTION ASSEMBLY
16	CLAMP, Cable	33	PAD, Lifter, nylon
17	PHOTOSENSE HEAD ASSEMBLY	34	TRANSFORMER ASSEMBLY
18	READ PREAMPLIFIER ASSEMBLY	35	CONTROL AND STATUS ASSEMBLY
19	WRITE INTERCONNECT ASSEMBLY	36	COVER DOOR INTERLOCK SWITCH ASSEMBLY (not shown)
20	MAGNETIC TAPE HEAD ASSEMBLY	37	SWITCH, Power, DPST, CAP, Protective
21	DENSITY SELECT SWITCH ASSEMBLY		
22 or	UNIT SELECT SWITCH ASSEMBLY		

to the standard manual.

The serial number plate contains a nine-digit, one-letter serial number (0000A00000). The first four digits are a serial number prefix indicating design changes. The letter designates the country in which the tape unit was manufactured ("A" indicates the United States). The remaining five digits are a sequential suffix that changes with each unit shipped by Hewlett-Packard. If the serial number prefix on the tape unit does not agree with the number of the title page of this manual, there are differences between the tape unit and the informatin contained in this manual. These differences are described in manual supplements which accompany this manual. These supplements are also available at the nearest HP Sales and Service Offices which are listed at the back of this manual.

Printed circuit assemblies (PCA) are identified by a letter, a series code, and a division code stamped or etched on the assembly (e.g. A-1535-46). The letter identifies the revision of the etched trace pattern on the unloaded printed circuit board. The four-digit series code pertains to the electrical characteristics of the loaded PCA and the positions of the components. The division code identifies the Hewlett-Packard division that manufactured the PCA.

1-4. OPTIONS.

Certain options for the tape unit are field installable but are usually installed at the factory at the time of purchase. Standard configuration option numbers are listed in table 1-1. Elective option numbers are listed in table 1-2.

1-5. CONTROL ASSEMBLIES.

Control assemblies (including options) consist of the control switch assembly, density select switch assembly, control and status printed circuit assembly (PCA), write enable assembly, the photosense head assembly unit select assembly, and for 7970E-parity select switch assembly. Refer to figures 1-2 and 1-3 for locations of these assemblies. Refer to parts and diagrams manual for switch configurations and locations. (Page 2-7 and 2-8).

1-6. CONTROL SWITCH ASSEMBLY.

The control switch assembly contains the front panel controls and indicators for controlling tape movement and indicating tape unit status. These are the RESET, REWIND, ON-LINE, and LOAD switches and indicators, and the WRITE ENABLE indicator (only on read/write units).

1-7. DENSITY SELECT SWITCH ASSEMBLY.

Density select is an optional feature which is applicable to the read/ write function. Standard units are hard wired to read or write at a tape packing density of 800 (7Tr., 9Tr. NRZI) or 1600 (9Tr PE) CPI. Density select allows selecting as follows:

	SWITCH DEPRESSED	FORMAT
a.	200 cpi	7 Tr NRZI
b.	556 cpi	7 Tr NRZI
c.	800 cpi	7 Tr, 9 Tr NRZI
d.	1600 cpi (multiformat 'E' only)	9 Tr PE

1-8. UNIT SELECT SWITCH ASSEMBLY.

Unit select is an optional feature for selecting and indicating an address when two to four tape units are connected to one controller. Standard tape units have a jumper located on the control and status PCA for addressing purposes.

1-9. PARITY SELECT SWITCH ASSEMBLY (7970E MULTIFORMAT ONLY).

The parity select option allows selecting and indicating either odd or even parity in seven track tape units.

1-10. CONTROL AND STATUS PCA.

This assembly serves as an interface between the transport assemblies, the read and write assemblies, the control switches, and the controller. It contains the logic which indicates the tape position, tape motion, and write status to the controller and other tape unit assemblies. It inhibits operation of the read and write circuits except under selected tape movement conditions, converts tape movement commands from the control switch assembly and the controller into tape movement signals to the capstan servo, and inhibits tape unit operation on command from the controller.

1-11. WRITE ENABLE ASSEMBLY.

The write enable assembly (used only on read/write tape units) consists of an activator, two microswitches, and a solenoid. It enables the tape unit for a write mode if write enable ring is installed on the supply reel before installing the reel on the reel hub. For read-only operation the ring is removed, resulting in a file protect status. This prevents data from inadvertently being written on the tape during a read operation.

1-12. PHOTOSENSE HEAD ASSEMBLY.

The photosense head assembly consists of a lamp and two phototransistors mounted near the magnetic tape heads. A Load Point or End-of-Tape signal to the control and status assembly is generated when the reflective tape markers indicating the beginning of tape (BOT or Load Point), end-of-tape (EOT) pass the photosense head assembly.

1-13. TRANSPORT ASSEMBLIES.

The tape transport assemblies consist of the capstan servo PCA and the capstan motor which move the tape; and supply and takeup reel servo PCA's, rell motors, and tension arm assemblies which form a servo system used to maintain tape tension. Refer to figure 1-2 for locations of these assemblies.

1-14. CAPSTAN SERVO PCA AND CAPSTAN MOTOR.

The capstan servo PCA contains logic and amplifiers for driving the capstan motor which moves the tape. It receives tape speed and direction commands from the control and status PCA. Three tape movement switches are located on the capstan servo PCA; the normal (synchronous) speed reverse switch, the synchronous speed forward switch, and the high speed (160 ips) forward switch. These switches are used for testing purposes to control forward and reverse tape movement at synchronous and high speeds.

1-15. TENSION ARM ASSEMBLIES.

The supply and takeup tension arm assemblies are identical. Each is composed of a spring loaded tension arm and a photoconductor circuit which converts the position of the tension arm into an electrical signal. Since the tension arms are spring loaded, the position of a tension arm is an indication of the amount of tape tension. The tension arm position signals are supplied to the reel servo PCA.

1-16. REEL SERVO PCA AND REEL MOTORS.

The reel servo PCA contains two circuits which amplify the signals from the supply and takeup tension arm assemblies. The amplified signals drive the supply and takeup reel motors to cause the tension arms to assume the desired position to maintain proper tape tension.

1-17. MAGNETIC TAPE HEAD ASSEMBLY.

The head assembly (depending upon options) consists of a write head stack, read head stack, erase head, two tape guides, crosstalk shield head gate, tape cleaner, and base plate (figure 1-4). The two tape guides ensure proper positioning and control of tape as it passes over the heads. Before reaching the heads, tape passes over a slotted, block type cleaner which removes any foreign particles. To assure high reliability recording, tape is erased by a high density, full-tape-width erase head.

The write/read heads are seven or nine track, NRZI and/or P.E. standard format which will handle tape packing densities of 200, 556, 800, or 1600 cpi with a tape speed range of 25 to 45 ips. A crosstalk shield head gate, positioned directly over the write/read heads, reduces write head to read head crosstalk during a write operation.

Channel scrambling is accomplished in the head cable. From the reference edge (edge

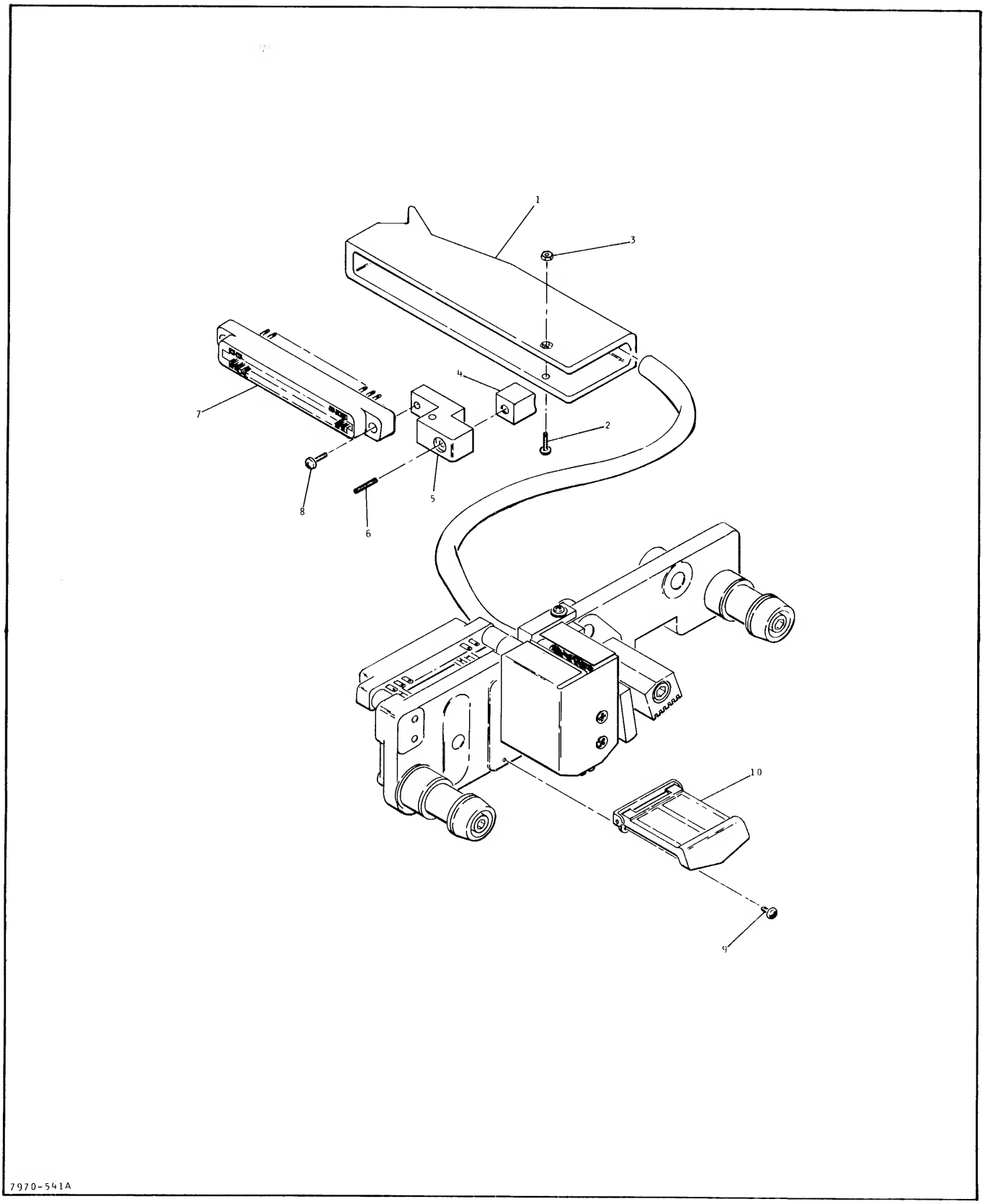


Figure 1-4. Magnetic Tape Head Assembly

facing the operator), the nine-track channel designations are 5, 7, 3, P, 2, 1, 0, 6, and 4. Seven-track channel designations from the reference edge are 7, 6, 5, 4, 3, 2, and P. The track channel designations are industry compatible.

1-18. READ ASSEMBLIES.

The read assemblies consist of a read preamplifier PCA, a card cage assembly (motherboard), a read control PCA, a single channel read data PCA, and three or four dual channel read data PCA's for seven-or nine-track operation, respectively. Refer to figures 1-2 and 1-3 for locations of these assemblies.

1-19. READ PREAMPLIFIER PCA.

The read preamplifier PCA contains nine identical amplifier circuits, one for each tape track. It amplifies the signals from the tape heads before they are applied to the read data and read control PCA's. Seven-track tape units have two unused channels (0, 1). The gain of each preamplifier is adjustable.

1-20. READ MOTHERBOARD ASSEMBLY.

The read motherboard assembly contains wiring for interconnecting the read preamp, read control and read data cards, and for interfacing with external circuits. 7970E slave units have a slave read assembly instead and the outputs go to the master unit read motherboard.

1-21. READ CONTROL PCA.

The read control PCA consists of circuits which control operation of the read data PCA's by establishing bias levels, providing voltage for read data skew delay circuits, and providing pulses used by the read data circuit to sample its output register.

1-22. READ DATA PCA'S.

The read data PCA's detect flux transitions in each track and produce a parallel digit output. This data is transferred to the output registers to provide the interface with a read data bit. Skew delay circuits compensate for nonperfect alignment of individual track gaps in the read head (gap scatter).

1-23. DECODER PCA

(7970E). The decoder PCA's decode the PE data (separate data from phase correction signals and noise). The track error detection takes place here also.

1-24. DATA AND STATUS PCA.

The data and status PCA uses sync pulses developed from the data flow to generate a clock DF (DF = data frequency) and 40DF signal, these signals are used for timing throughout data flow. It also gives data status (i.e., do we have data?, do we have parity?) and contains the threshold generator.

1-25. WRITE ASSEMBLIES.

The write assemblies consist of a write interconnect assembly, card cage assembly (motherboard), a write control PCA, a single channel write data PCA, and three or four dual channel write data PCA's for seven- or nine-track operation respectively. Refer to figures 1-2 and 1-3 for location of these assemblies.

1-26. WRITE MOTHERBOARD ASSEMBLY.

The write motherboard assembly contains wiring for connecting the write control PCA and the write data PCA's to the write head. It also interfaces the write circuits with external circuits.

1-27. WRITE INTERCONNECT PCA.

The write interconnect PCA contains load resistors for all write drivers. It interconnects the head assembly with the write assembly and is located near the head assembly.

1-28. WRITE CONTROL PCA.

The write control PCA processes tape unit motion status signals and interface commands to control the write data circuits. When unit write condition is first established, the write control circuits ensure that the write head drivers are in a reset state (inter-record gap flux) and tape is saturated in the same polarity as the erase head.

1-29. WRITE DATA PCA'S.

The write data PCA's contain skew delay circuits to compensate for write head gap scatter and write head drivers which saturate the write heads for flux reversals.

1-30. POWER DISTRIBUTION ASSEMBLY.

The power distribution assembly consists of a transformer assembly, a power distribution PCA, and a power regulator PCA. The bottom section of the tape unit housing rear panel may be removed to gain access to the power supply components. Refer to figure 1-3 for locations of these assemblies.

1-31. TRANSFORMER ASSEMBLY.

The transformer assembly consists of a metal panel upon which are mounted the primary fuses, the 115V/230V switch for power source selection, a filter, the transformer, and three bridge rectifier circuits.

1-32. POWER DISTRIBUTION PCA.

The power distribution PCA contains the secondary fuses, filter capacitors and resistors, diodes, and three series regulator power transistors mounted on a heat sink. (5 power transistors on 7970E Master Tape Drives).

1-33. POWER REGULATOR PCA.

The power regulator PCA contains components for three regulator circuits which control current through the +12 volt, -12 volt, and -5 volt series regulator transistors. It also contains circuits for supplying additional power to the reel servo circuits under conditions of high speed forward and reverse tape movement.

1-34. SPECIFICATIONS.

Specifications of the tape unit equipped with read and write modules and all available options are listed in table 1-3.

1-35. ACCESSORIES FURNISHED.

The following accessories are furnishable with the standard tape unit.

Part No.	Description	Qty.
07970-00580	Rack Mounting Bracket	1
2190-0034	Lockwasher, no. 10	7
2680-0103	Screw, no. 10-32, 0.5 inch	7
2680-0116	Screw, no. 10-32, 0.375 inch.	4
3050-0002	Washer, Flat	7
8120-1348	AC Power Cable	1
1490-0738	Magnetic Tape Reel	1

1-36. ACCESSORIES AVAILABLE.

The following accessories are available for the tape unit at extra cost.

a. HP 13190A Multiunit Cable (12.5 feet).

b. HP 13190B Multiunit Cable (20 feet).

c. Transport Test Tape, part number 5080-4525 (for seven track application).

d. Transport Test Tape, part number 5080-4526 (for nine track application).

e. 200 BPI Reference Amplitude Test Tape, part number 5080-4547 (for read only systems).

f. Write Test Tape, part number 9162-0025 (standard computer grade tape: 3M 777 or Memorex MRX 111 on 10.5 inch reels).

g. Master Alignment Tape, part number 9162-0027.

h. HP 13191A Control and Status Test Board.

i. HP 13192A Write Test Board.

j. HP 13193A Read Test Board.

k. HP 13012B Read Parity for seven- and nine-tracks.

l. HP 13014A Write Parity for nine track.

m. HP 13014A-001 Write Parity for seven track.

n. Rack Mounting Kit, part number 07970-62118.

o. HP 13016A TMZ Adapter Kit.

p. HP 13017A PEC Adapter Kit.

1-37. RELATED MANUALS.

Manuals containing information pertinent to the HP 7970B/7970E Digital Magnetic Tape Unit are as follows:

a. HP 7970 B/C/E Operator Manual, part number 07970-90885.

b. 7970 B/C/E Schematic Manual, part number 07970-90886.

c. HP 13012B Programmable Read Parity Accessory Manual, part number 13012-90003.

d. HP 13190A/B Multiunit Cable Accessory Kit Manual, part number 13190-90012.

e. HP 13191A Control and Status Test Accessory Manual, part number 13191-90000.

f. HP 13192A/13193A Write Test and Read Test Accessory Kit Manual, part number 13192-90002.

g. HP 13016A Interface Adapter Kit Manual, part number 13016-90001.

h. HP 13017A Interface Adapter Kit Manual, part number 13017-90001.

Table 1-4. Specifications, Magnetic Tape Unit 7970B

TAPE SPEED
25.0 ips, 37.5 ips, 45 ips

REEL DIAMETER
Up to 10.50 inches (26.7 cm)

TAPE (Computer Grade)
Width: 0.5 inches (1.3 cm)
Thickness: 1.5 mils min

TAPE TENSION
8.5 oz, nominal (.240 kg)

FAST FORWARD/REWIND SPEED
160 ips (4.06 m/sec)

INSTANTANEOUS SPEED VARIATION
±3% (measured bit-to-bit)

LONG-TERM SPEED VARIATION
±1%

FAST FORWARD, FAST REVERSE, START/STOP CHARACTERISTICS
Distance: 40 inches, nominal start (25 ips)
69 inches, nominal start (37.5 and 45 ips)
31 inches, nominal stop (37.5 and 45 ips)

Time: 0.7 second, maximum

START/STOP TAPE TRAVEL
0.187±0.020 inch (.476±0.05 cm)

REEL MOTOR BRAKING
Dynamic

RECORDING MODE
NRZI (industry compatible)

MAGNETIC HEAD ASSEMBLY
Standard: seven- or nine-track, erase, write and read
Gap Scatter (Measured Optically):
Read Stack: 150 microinches, maximum
Write Stack: 150 microinches, maximum

SKEW
Static Skew: The per channel delayed one-shot deskewing technique is utilized in the write (forward) and read (forward and reverse) circuitry effectively eliminating static skew.
Dynamic Skew: ±200 microinches (read after write), maximum

POWER REQUIREMENTS
115 or 230 (±10%) Vac, Switch Selectable
48 to 66 Hz, single phase
400 VA, maximum (on high line)

WRITE HEAD TO READ HEAD CROSSTALK
5% (of read signal)

READ HEAD CHANNEL TO READ HEAD CHANNEL CROSSTALK
-30 dB

BEGINNING-OF-TAPE AND END-OF-TAPE REFLECTIVE STRIP DETECTION
Photoelectric, industry compatible

OPERATING ENVIRONMENT
Ambient Temperature: +32° to +131°F (0° to 55°C)
Relative Humidity: 20 to 80% (non-condensing)
Altitude: 10,000 ft (3.048 m)
Heat Dissipation 1400 BTU

START/STOP TIMES
15 ms (at 25 ips)
10 ms (at 37.5 ips)
8.33 ms (at 45 ips)

DIMENSIONS
Height: 24 inches (61 cm)
Width: 19 inches (48.3 cm)
Depth: 12 inches (30.5 cm)
Overall Depth: 15.875 (40.3 cm)

WEIGHT
130 lb maximum (59.02 kilograms)

TRANSPORT MOUNTING
Vertical: Standard 19 inches (48.3 cm) Retma rack

HEAD GUIDE SPACING
Industry Campatible

Table 1-5. Specifications, Magnetic Tape Unit 7970E

TAPE SPEED
22.5 ips, 25 ips, 37.5 ips, and 45 ips

REEL DIAMETER
Up to 10.50 inches (26.7 cm)

TAPE (Computer Grade)
Width: 0.5 inches (1.3 cm)
Thickness: 1.5 mils

TAPE TENSION
8 oz, nominal (.240 kg)

FAST FORWARD/REWIND SPEED
160 ips (4.06 m/sec)

INSTANTANEOUS SPEED VARIATION
±3% (measured bit-to-bit)

LONG-TERM SPEED VARIATION
±1%

FAST FORWARD, FAST REVERSE, START/STOP CHARACTERISTICS
Distance: 40 inches, nominal start (25 ips)
69 inches, nominal start (37.5 and 45 ips)
31 inches, nominal stop (37.5 and 45 ips)

Time: 0.7 second, maximum

START/STOP TIMES
15 ms (at 25 ips)
10 ms (at 37.5 ips)
8.33 ms (at 45 ips)

START/STOP TAPE TRAVEL
0.187 ± 0.020 inch (0.476 ± 0.05 cm)

REEL MOTOR BRAKING
Dynamic

MAGNETIC HEAD ASSEMBLY
Standard: Seven- or nine-track, erase, write and read
Gap Scatter (Measured Optically):
Read Stack: 150 microinches, maximum
Write Stack: 150 microinches, maximum

POWER REQUIREMENTS
115 or 230 (±10%) Vac
50 to 66 Hz, single phase
400 VA, maximum (on high line)

RECORDING MODE
Phase Encoding (PE) (Industry compatible)

SKEW
Static skew adjustable for write circuitry only.

HEAD GUIDE SPACING
Industry compatible

WRITE HEAD TO READ HEAD CROSSTALK
5% (of read signal)

READ HEAD CHANNEL TO READ HEAD CHANNEL CROSSTALK
-30 dB

BEGINNING-OF-TAPE AND END-OF-TAPE REFLECTIVE STRIP DETECTION
Photoelectric, Industry compatible

OPERATING ENVIRONMENT
Ambient Temperature: +32° to +131°F (0° to 55°C)
Relative Humidity: 20 to 80% (non-condensing)
Altitude: 10,000 ft (3.05 kilometer)
Heat Dissapation 1400 BTU

DIMENSIONS
Height: 24 inches (61 cm)
Width: 19 inches (48.3 cm)
Depth: 12 inches (30.5 cm) from mounting surface)
Overall Depth: 15.875 inches (40.3 cm)

WEIGHT
140 lb maximum (63.56 kilograms)

TRANSPORT MOUNTING
Vertical: Standard 19 inches (48.3 cm) Retma Rack

7970B/7970E MNEMONICS

Table 1-5 lists the mnemonics used in the 7970B/E service manual and diagrams manual. Some of the mnemonics are prefaced with an "L" (ie, LEVEN on the data and status PCA). This signal represents $\overline{\text{EVEN}}$. The "L" stands for "low" or "not". This method is used to code signals for computers since a bar (XXXX) is not recognized by the computer.

Table 1-6. List of Mnemonics

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
AC	Amplitude comparison	REV	Reverse tape motion
ALL	All nine LV signals active	REV 0	Reverse tape motion (master)
ANYL	Any LV signal active	REV 1	Reverse tape motion (slave)
CF	Forward tape motion command	SB	Skew buffer bit
CH	High-speed tape motion command	SBEZ	Skew buffers equal zero (bits stored in all nine skew buffers are logic 0's)
CL	Off-line command		
CLRG	Clear error-correction and output registers		
CR	Reverse tape motion command	SD2	Density 200 status
CRW	Rewind command	SD5	Density 556 status
CS 0	Select unit 0	SD8	Density 800 status
CS 1	Select unit 1	SD16	Density 1600 status
CS 2	Select unit 2	SET	End of tape status
CS 3	Select unit 3	SFP	File protect status
DF	Data frequency	SL	On-line status
40 DF	A frequency forty times greater than DF	SLP	Load point status
DRDY	Data ready	SOLA	Select on-line A
D16	Density 1600 selected	SOLB	Select on-line B
EOB	End of block	SPE	Slave PE read status
EOD	End of data	SR	Ready status
EP	Even parity	SRW	Rewind status
EVEN	Uncorrectable error	STE	Single-track error
EWL	Enable window logic	S7T	Seven-track status
E1	One channel in error	+TH	Positive threshold
FWD	Forward tape motion	-TH	Negative threshold
GE2	More than one channel in error	TIE	Track in error
HSFWD	High-speed forward tape motion	TM	Tape mark (or file mark)
HSREV	High-speed reverse tape motion	TML	Tape mark level
IDB	Identification burst	WD	Write data bit
IDL	Identification level	WL	Write latch
IPA	Increment pointer address	WSW	Write command
LV	Level (signal present)	WS1	Slave PE write status
MREN	Master tape unit read enable	XEC	Error-correction register store command
MREV	Master tape unit reverse tape motion	XEN	Enable master PE read circuits output signals
MTE	Multiple track error	XOR	Output buffer register store command
RC	Read clock	ZX	Zero crossing
RD	Read data bit	40 DF	A frequency forty times greater than DF

INSTALLATION

SECTION II

2-1. INTRODUCTION.

This section contains installation information and information pertaining to unpacking, inspection, claims for damage, site selection, and reshipping procedures.

2-2. SITE SELECTION.

The tape unit is designed for operation at sites that are not subject to excessive shocks, excessive vibration, or wide ranges of ambient temperatures. The unit should be located to provide access to both front and rear sections of the cabinet with sufficient room for the maximum swing radius of the cover door and the main casting door. Convection cooling is provided by perforated top, bottom, and rear lower panels. No forced air ventilation is required where the exterior ambient temperature does not exceed 131^{o}F and no other heat generating equipment is housed in the cabinet.

2-3. UNPACKING AND INSPECTION.

If the shipping carton is damaged upon receipt, requiest that the carrier's agent be present when the unit is unpacked. Inspect the unit for damage (caracks, broken parts, etc.). If the unit is damaged and fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual). Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged unit without waiting for any claims against the carrier to be settled.

When unpacking the unit, retain all packing materials and hardware for future use. The following procedures describe how to unpack the unit in order to save all packing materials.

a. Using a sharp knife or similar tool, cut the top seal of the outer shipping box.

b. Remove the six toro pads isolating the inner shipping box.

c. Cut the top seal of the inner shipping box and remove accessory cartons or filler cartons.

d. Remove accessory liner and top pad.

e. Remove plastic sheet from face of unit.

CAUTION

The unit weighs up to approximately 140 pounds (63.56 kg). Two persons are required to lift the unit from the ship ping container.

f. Remove unit from inner shipping box.

g. Remove the two number 10-32 screws and washers that secure the right-hand side of tape unit door casting to the housing.

2-4. INSTALLATION.

Installation of the tape unit is limited to mounting the unit in a standard 19-inch rack and connecting interface cabling. The following procedures describe the installation of the unit in a 19-inch rack.

CAUTION

The weight of the transport in the open position must be considered and ballast may be required to prevent the rack from tipping forward.

a. Remove protective covering from accessory kit and locate four number 10-32 flat head screws (part number 2680-0116) and rack mounting bracket (part number 07970-00580).

b. Attach the rack mounting bracket to the left rail of the rack with the four number 10-32 flat head screws. Orient the rack mounting bracket so that the upper and lower flanges face the inside of the rack. These flanges form a cradle to hold the left (hinged) side of the tape unit.

c. Place the tape unit into position and using three number 10-32, 0.5-inch machine screws (part number 2680-0103), three flat washers, and three lockwashers, attach the right side of the transport housing to the 19-inch rack.

d. Using the remaining four number 10-32, 0.5-inch machine screws (part number 2680-0103), flat washers and lockwashers, secure the left side of the transport housing to the rack mounting bracket.

WARNING

The tape unit power cable is equipped with a three-wire connector. Do not defeat the ground connection by using an adapter or breaking the grounding pin of the connector. Isolating the unit from ground creates a hazardous condition which may result in death or serious injury.

e. Connect the female polarized connector of power cable W1 to the male power connector of the tape unit. Route the power cable to the site power outlet.

2-5. CABLES AND CONNECTORS.

There are three interface mating connectors. Each is specifically associated with one function as listed below:

a. Control and Status.

b. Write Data.

c. Read Data.

The male portions of these connectors are presented to the interface cables, via supplied mating connectors, as etched sections of printed-circuit assemblies. These assemblies are located within the rear section of the tape unit (figure 1-3).

Three female mating connectors are supplied; each has a 48-pin (24 active line) capability. These mating connectors are intended to be directly connected to the users interfacing cables. Strain relief hardware is also provided. Tables 2-1, 2-2, and 2-3 list the pin assignments and line names. These lines are described in tables 2-4, 2-5, 2-6, 2-7, and 2-8.

Table 2-1. Control and Status Connector

ACTIVE PIN	GROUND PIN	SIGNAL NAME	MNEMONICS
1X (A)	1	$\overline{\text{On-Line Status}}$	$\overline{\text{SL}}$
2X (B)	2	$\overline{\text{Load Point Status}}$	$\overline{\text{SLP}}$
3X (B)	3	$\overline{\text{Rewind Status}}$	$\overline{\text{SRW}}$
4X (D)	4	$\overline{\text{End-of-Tape Status}}$	$\overline{\text{SET}}$
5X (E)	5	$\overline{\text{Ready Status}}$	$\overline{\text{SR}}$
6X (F)	6	$\overline{\text{File Protect Status}}$	$\overline{\text{SFP}}$
7X (H)	7	$\overline{\text{Density 800 Status}}$	$\overline{\text{SD8}}$
8X (J)	8	$\overline{\text{Density 556 Status}}$	$\overline{\text{SD5}}$
9X (K)	9	$\overline{\text{Density 200 Status}}$	$\overline{\text{SD2}}$
10X (L)	10	$\overline{\text{Select Unit 3}}$	$\overline{\text{CS3}}$
11X (M)	11	$\overline{\text{Select Unit 2}}$	$\overline{\text{CS2}}$
12X (N)	12	$\overline{\text{Select Unit 1}}$	$\overline{\text{CS1}}$
13X (P)	13	$\overline{\text{Select Unit 0}}$	$\overline{\text{CS0}}$
14X (R)	14	$\overline{\text{Rewind Command}}$	$\overline{\text{CRW}}$
15X (S)	15	$\overline{\text{Off-Line Command}}$	$\overline{\text{CL}}$
16X (T)	16	$\overline{\text{Forward Command}}$	$\overline{\text{CF}}$
17X (U)	17	$\overline{\text{Reverse Command}}$	$\overline{\text{CR}}$
18X (V)	18	$\overline{\text{High-Speed Command}}$	$\overline{\text{CH}}$
19X (W)	19	$\overline{\text{Set Write Command}}$	$\overline{\text{WSW}}$
20X (X)	20	Reserved for Options and Spares	–
through	through	↕	
24X (BB)	24	Reserved for Options and Spares	–

Table 2-2. Write Data Connector*

ACTIVE PIN	GROUND PIN	SIGNAL NAME	MNEMONICS
1X (A)	1	Reserved for Options	–
2X (B)	2	↕	–
3X (C)	3		–
4X (D)	4		–
5X (E)	5	Reserved for Options	–
6X (F)	6	$\overline{\text{Write Status}}$	$\overline{\text{SW}}$
7X (H)	7	Reserved for Options	–
8X (J)	8	Write Clock	WC
		IBM DESIGNATIONS (NINE-TRACK ONLY)	
9X (K)	9	Write Data P	WDP
10X (L)	10	Write Data 0	WD0
11X (M)	11	Write Data 1	WD1
12X (N)	12	Write Data 2	WD2
13X (P)	13	Write Data 3	WD3
14X (R)	14	Write Data 4	WD4
15X (S)	15	Write Data 5	WD5
16X (T)	16	Write Data 6	WD6
17X (U)	17	Write Data 7	WD7
18X (V) through 24X (BB)	18 through 24	Reserved for Options and Spares ↕ Reserved for Options and Spares	– –

*Used only in PE read-after-write.

Table 2-3. Master PE Read Data Connector

ACTIVE PIN	GROUND PIN	SIGNAL NAME	MNEMONICS
1X (A)	1	Reserved for Options and Spares	–
2X (B)	2	↕	–
3X (C)	3		–
4X (D)	4		–
5X (E)	5		–
6X (F)	6		–
7X (H)	7	Reserved for Options and Spares	–
8X (J)	8	$\overline{\text{Read Clock}}$	$\overline{\text{RC}}$
		IBM DESIGNATIONS (NINE-TRACK ONLY)	
9X (K)	9	$\overline{\text{Read Data P}}$	$\overline{\text{RDP}}$
10X (L)	10	$\overline{\text{Read Data 0}}$	$\overline{\text{RD0}}$
11X (M)	11	$\overline{\text{Read Data 1}}$	$\overline{\text{RD1}}$
12X (N)	12	$\overline{\text{Read Data 2}}$	$\overline{\text{RD2}}$
13X (P)	13	$\overline{\text{Read Data 3}}$	$\overline{\text{RD3}}$
14X (R)	14	$\overline{\text{Read Data 4}}$	$\overline{\text{RD4}}$
15X (S)	15	$\overline{\text{Read Data 5}}$	$\overline{\text{RD5}}$
16X (T)	16	$\overline{\text{Read Data 6}}$	$\overline{\text{RD6}}$
17X (U)	17	$\overline{\text{Read Data 7}}$	$\overline{\text{RD7}}$
18X (V)	18	$\overline{\text{Density 1600}}$	$\overline{\text{SD16}}$
19X (W)	19	Reserved for Options and Spares	–
20X (X)	20	$\overline{\text{Multiple Track Error}}$	$\overline{\text{MTE}}$
21X (Y)	21	$\overline{\text{Tape Mark}}$	$\overline{\text{TM}}$
22X (Z)	22	$\overline{\text{Single Track Error}}$	$\overline{\text{STE}}$
23X (AA)	23	$\overline{\text{ID Burst}}$	$\overline{\text{IDB}}$
24X (BB)	24	$\overline{\text{End-of-Block}}$	$\overline{\text{EOB}}$

Table 2-4. NRZI Read Data Connector

ACTIVE PIN	GROUND PIN	SIGNAL NAME		MNEMONICS	
1X (A)	1	$\overline{\text{Even Parity Selected}}$		$\overline{\text{EP}}$	
2X (B)	2	Reserved for Options and Spares		–	
3X (C)	3	Reserved for Options and Spares		–	
4X (D)	4	Reserved for Options and Spares		–	
5X (E)	5	$\overline{\text{Status Seven Track}}$		$\overline{\text{S7T}}$	
6X (F)	6	Reserved for Options and Spares		–	
7X (H)	7	Reserved for Options and Spares		–	
8X (J)	8	Read Clock		RC	
		IBM DESIGNATIONS			
		(NINE-TRACK)	(SEVEN-TRACK)	(NINE-TRACK)	(SEVEN-TRACK)
9X (K)	9	Read Data P	Read Data C	RDP	RDC
10X (L)	10	Read Data 0	–	RD0	–
11X (M)	11	Read Data 1	–	RD1	–
12X (N)	12	Read Data 2	Read Data B	RD2	RDB
13X (P)	13	Read Data 3	Read Data A	RD3	RDA
14X (R)	14	Read Data 4	Read Data 8	RD4	RD8
15X (S)	15	Read Data 5	Read Data 4	RD5	RD4
16X (T)	16	Read Data 6	Read Data 2	RD6	RD2
17X (U)	17	Read Data 7	Read Data 1	RD7	RD1
18X (V) through 24X (BB)	18 through 24	Reserved for Options and Spares ↕ Reserved for Options and Spares		– –	

Table 2-5. Slave PE Read Data Connector

ACTIVE PIN	GROUND PIN	SIGNAL NAME	MNEMONICS
1X (A)	1	Zero Crossing Data P	ZXP
2X (B)	2	Amplitude Comparator Data P	ACP
3X (C)	3	Zero Crossing Data 0	ZX0
4X (D)	4	Amplitude Comparator Data 0	AC0
5X (E)	5	Zero Crossing Data 1	ZX1
6X (F)	6	Amplitude Comparator Data 1	AC1
7X (H)	7	Zero Crossing Data 2	ZX2
8X (J)	8	Amplitude Comparator Data 2	AC2
9X (K)	9	Zero Crossing Data 3	ZX3
10X (L)	10	Amplitude Comparator Data 3	AC3
11X (M)	11	Zero Crossing Data 4	ZX4
12X (N)	12	Amplitude Comparator Data 4	AC4
13X (P)	13	Zero Crossing Data 5	ZX5
14X (R)	14	Amplitude Comparator Data 5	AC5
15X (S)	15	Zero Crossing Data 6	ZX6
16X (T)	16	Amplitude Comparator Data 6	AC6
17X (U)	17	Zero Crossing Data 7	ZX7
18X (V)	18	Amplitude Comparator Data 7	AC7
19X (W)	19	Reserved for Options and Spares	–
20X (X)	20	Reserved for Options and Spares	–
21X (Y)	21	Reserved for Options and Spares	–
22X (Z)	22	$\overline{\text{Write Status}}$	$\overline{\text{WS1}}$
23X (AA)	23	$\overline{\text{Reverse}}$	$\overline{\text{REV1}}$
24X (BB)	24	$\overline{\text{Phase-Encode Status}}$	$\overline{\text{SPE}}$

Table 2-6. Detailed Description of I/O Lines, Control and Status Connector

I/O LINE	DESCRIPTION	SIGNAL TYPE	SIGNAL DIRECTION
STATUS			
a. ON-LINE (SL = STATUS ON-LINE)	Acknowledges that the selected tape unit has been manually placed in an on-line condition.	Level	Output
b. READY (SR = STATUS READY)	Indicates that the tape unit is selected, is on-line, the initial loading sequence is complete, and the tape unit is not rewinding.	Level	Output
c. LOAD POINT (SLP = STATUS LOAD POINT)	Indicates that the tape unit is selected, is on-line, and the tape is positioned at the load point reflective strip.	Level	Output
d. DENSITY STATUS (SD = STATUS DENSITY) NOTE: Three individual lines SD2, SD5, and SD8	Indicates the manual setting of a tape unit density switch: 220, 556, 800 CPI. Only one density at a time can be asserted from a selected and on-line tape unit.	Level	Output
e. REWIND (SRW = REWIND STATUS)	Indicates that the selected and on-line tape unit is engaged in a rewind operation. This status remains true until the tape is positioned at the load point reflective strip.	Level	Output
f. FILE PROTECT (SFP = STATUS FILE PROTECT)	Indicates that the selected and on-line tape unit is not write enabled (write ring is not present in the file reel).	Level	Output
g. END-OF-TAPE (SET = STATUS END OF TAPE)	Indicates that an end-of-tape reflective strip has passed under the photosense head of a selected and on-line tape unit. Assertion is maintained until cancellation of the end-of-tape condition by the passage of the reflective strip in the reverse direction.	Level	Output
FUNCTION COMMANDS			
a. SELECT (CS = COMMAND SELECT) NOTE: Four individual lines for units 0, 1, 2, and 3	Selects a particular on-line tape unit from a group connected to a common interface cable.	Level	Input to tape unit
b. OFF-LINE (CL = COMMAND OFF-LINE)	Assertion of this line clears the write condition and terminates the on-line condition of the selected tape unit. Assertion should be maintained until acknowledged by the negation of the on-line status.	Level	Input to tape unit

Table 2-6 continued.

I/O LINE	DESCRIPTION	SIGNAL TYPE	SIGNAL DIRECTION
FUNCTION COMMANDS (Continued) c. SET WRITE (WSW = WRITE SET WRITE)	The assertion transition of CF causes the WSW line to be sampled following a 20 μs maximum delay period. Assertion transition of the WSW line enables the setting of the selected and on-line tape unit's write condition, provided the tape unit is ready and write enabled. Negation of the WSW line enables the clearing of the tape unit's write condition. The desired logic level of WSW shall be maintained for not less than 20 μs after the assertion edge of CF.	Level	Input to tape unit
MOTION COMMANDS a. FORWARD (CF = COMMAND FORWARD)	Providing the tape unit is selected, and ready, this command causes tape to be driven in the forward direction.	Level	Input to tape unit
b. REVERSE (CR = COMMAND REVERSE)	When asserted, clears the write condition and causes the tape to be driven in the reverse direction, provided that the tape unit is selected, and ready. Load point status inhibits the response to this command.	Level	Input to tape unit
c. REWIND (CRW = COMMAND REWIND)	Clears the write command on the selected tape unit and initiates a rewind operation, provided that the tape unit is ready, and not at load point. Tape is positioned at load point at the end of this operation. Assertion should be maintained until acknowledged by rewind status. (Minimum 2 μs.)	Level	Input to tape unit
d. HIGH SPEED (CH = COMMAND HIGH SPEED)	When asserted with forward or reverse on a selected and ready tape unit, will cause tape speed to accelerate to 160 ips.	Level	Input to tape unit

Table 2-7. Detailed Description of I/O Lines, Write Data Connector

I/O LINE	DESCRIPTION	SIGNAL TYPE	SIGNAL DIRECTION
STATUS a. WRITE STATUS (SW = STATUS WRITE)	Indicates that the selected tape unit is write enabled and current is flowing in the write and erase heads.	Level	Output from tape unit
DATA TRANSMISSION a. WRITE DATA (WD = WRITE DATA) WD0 thru WD7, WDP NOTE: Refer to write data connector for channel designation.	These lines (any one of nine lines) receive data to be recorded on tape as a character and must be electrically stable at assertion transition time of write clock and for 2 μs, minimum, thereafter.	Level	Input
b. WRITE CLOCK (WC = WRITE CLOCK)	The assertion transition of this pulse causes the character, represented by the write data lines, to be written on tape. The tape unit must be in the write condition and the assertion of the write clock must be maintained for a minimum of 2 μs.	Level	Input
c. WRITE RESET (WRS = WRITE RESET)	The assertion transition causes the LRCC character to be written on tape, provided the unit is in the write mode. Assertion must be maintained for a minimum of 2 μs.	Pulse	Input

Table 2-8. Detailed Description of I/O Lines, Read Data Connector

I/O LINE	DESCRIPTION	SIGNAL TYPE	SIGNAL DIRECTION
READ DATA TRANSMISSION a. READ DATA (RD = READ DATA) RD0 thru RD7, RDP NOTE: Refer to read data connector for channel designation.	These lines (any one of nine lines) detected characters read from the tape and present them to the interface. The read data lines are settled at the assertion transition time of read clock, and remain settled until 1 μs, maximum, before the next read clock.	Level	Output
b. READ CLOCK (RC = READ CLOCK)	Indicates that a character has been read from tape and is present on the read data lines. Assertion time is 2μs, minimum, 3μs, maximum.	Pulse	Output

The suggested maximum cable length is 20 feet from connector pin to connector pin. The interfacing cable should employ one set of twisted pairs for each input/output (I/O) line function, with one of the pair being used for the active I/O line, the other being used for terminal grounding at both ends of the cable to reduce the magnitude of intercable crosstalk. Unless otherwise specified, all wires should be 26 AWG, minimum, not less than one twist per inch, with a minimum insulation thickness of 0.01 inch. Figure 2-1 shows interface connector details and describes fabrication of an interface cable.

2-6. MULTIPLE UNIT INSTALLATION.

The control and status PCA, PE read motherboard PCA, PE write motherboard PCA, NRZI write motherboard PCA, and NRZI read motherboard PCA are manufactured with a concector paralleling the input/output connector to enable connection of test PCA's. The second connector also serves, in the case of the PE read circuits, to enable connection of tape units into master/slave configurations. Figures 2-2, 2-3, 2-4, 2-5, 2-6, and 2-7 show multiple unit installation of master/slave and master/master, and NRZI configurations. Figures 2-8, 2-9, and 2-10 show interface connectors of the tape units. The HP 13194A Multiunit Cable Accessory Kit Installation Manual gives additional information on multiple unit installtion. Up to four 7970B NRZI units can be connected to a common controller and each has its own address. A jumper on the control and status PCA in standard units or the unit select address switch on units with unit select option is used to establish the unit address. (0, 1, 2, or 3).

2-7. INPUT/OUTPUT LINE TRANSMITTERS AND RECEIVERS.

The tape unit interface I/o transmitter and receiver electrical parameters are shown and described in figure 2-11.

2-8. CHECKOUT PROCEDURES.

After the unit is installed and interface connections are completed, visually inspect the installation. Ensure that the power source is adequate and that all cables are properly anchored. Refer to section I for a description of all operating controls and indicators. Perform the initial mechanical check and checkout procedures described in section III to ensure that the unit is operational.

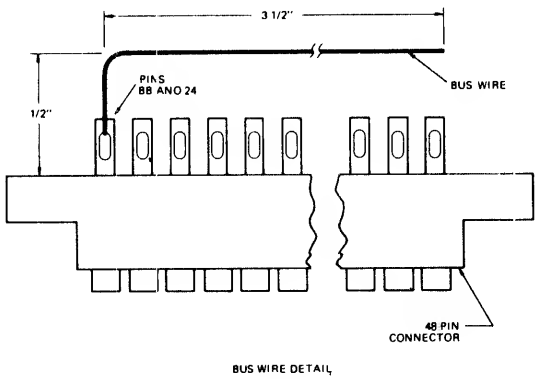
2-9. RESHIPMENT.

If the tape unit or any part of the unit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the information shown on the model plate and serial number of the unit. When packing the unit for shipment, observe the following precautions and use the original packing materials.

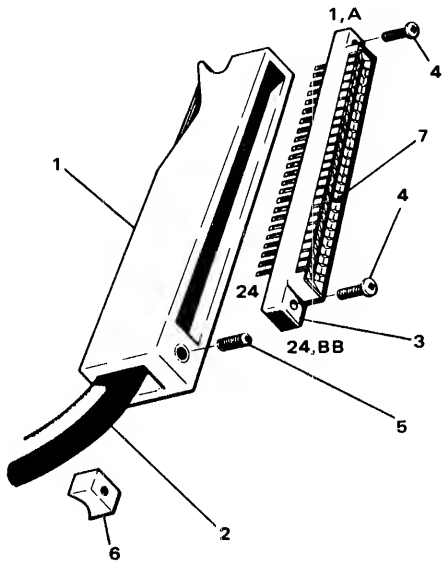
a. Ensure that the two number 10-32, 0.75-inch machine screws (part number

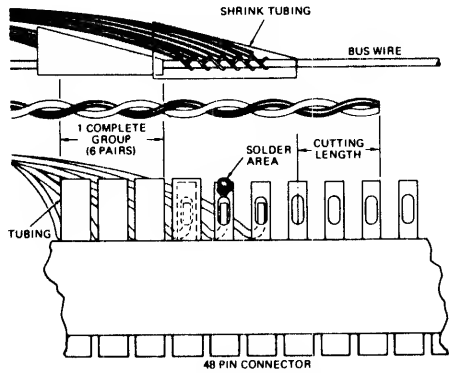
CABLE AND CONNECTOR PARTS

ITEM	DESCRIPTION	HP PART NO.
1	Connector hood	02116-4001
2	Cable, 24 twisted pair	8120-1700 or equivalent
3	Connector, 48-pin	1251-2518
4	Self-tapping screw	0624-0098
5	Setscrew	0624-0009
6	Cable clamp	02116-4003
7	Polarizing Key	1215-1115



BUS WIRE DETAIL





CABLE FABRICATION

To fabricate the interconnect cable refer to the above information and proceed as follows:

a. Insert approximately 10 inches of cable (2) into connector hood (1).

b. Strip the outer jacket of the cable back 5 inches.

c. Prepare a bus wire from 22-gauge bare-copper wire and solder it to pins BB and 24 of the connector (3) as shown in bus wire detail above.

d. Divide the 24 twisted pairs into groups of six pairs each.

e. Starting at the end of the 48-pin connector nearest pins BB and 24, connect the first six pairs as follows:

(1) Solder the six signal (white) wires to the respective pins on the connector and insulate each pin with shrink tubing as shown above.

(2) Solder the six ground (black) wires to the bus wire and insulate with shrink tubing as shown above.

f. Repeat steps (1) and (2) with the remaining groups of wires until all wires are soldered to the connector and insulated.

g. Trim off any excess bus wire and install the 48-pin connector (3) in the connector hood (1) using the two self-tapping screws (4).

h. Install cable clamp (6) and tighten in place with the setscrew (5).

7979-451

Figure 2-1. Interconnection Cable Fabrication

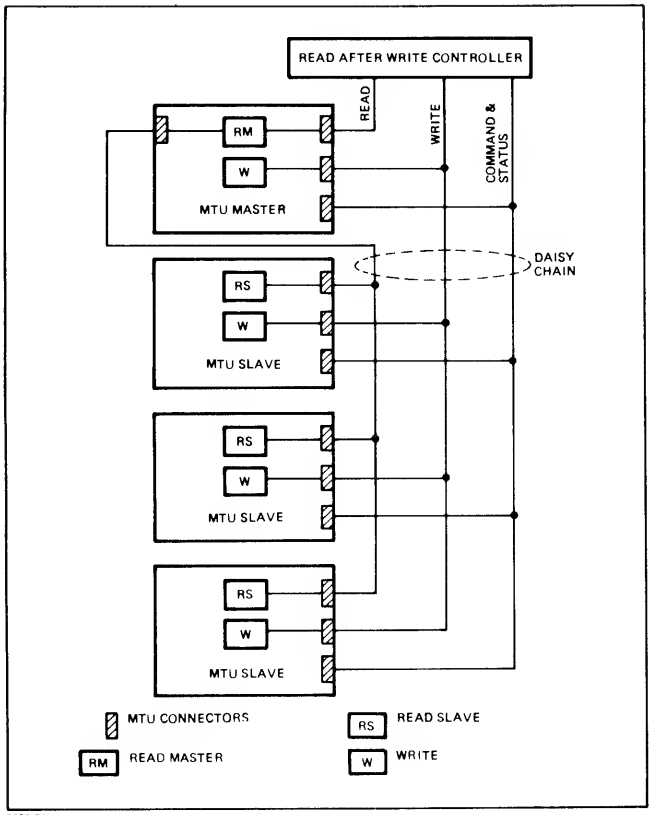


Figure 2-2. Read-After-Write, Master-to-Slave Configuration

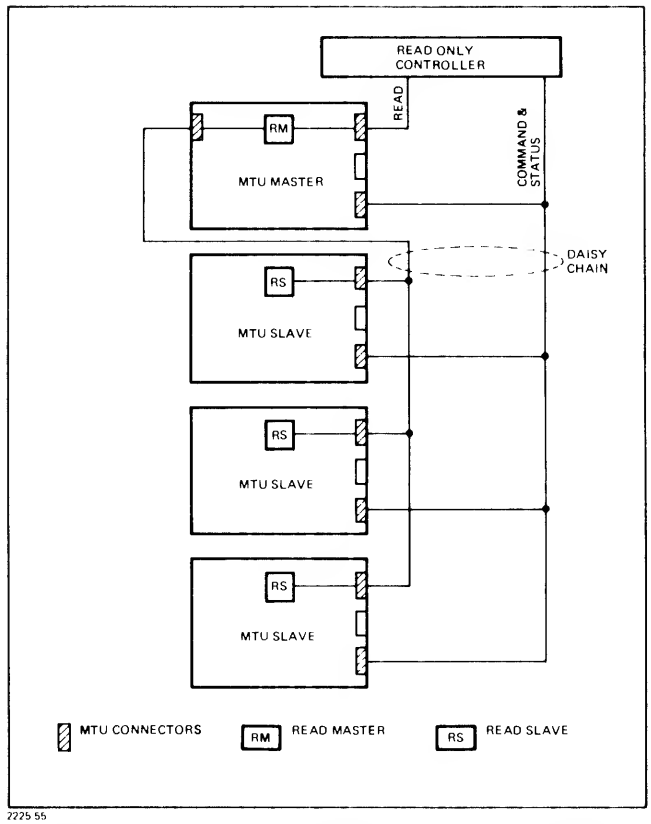


Figure 2-3. Read-Only, Master-to-Slave Configuration

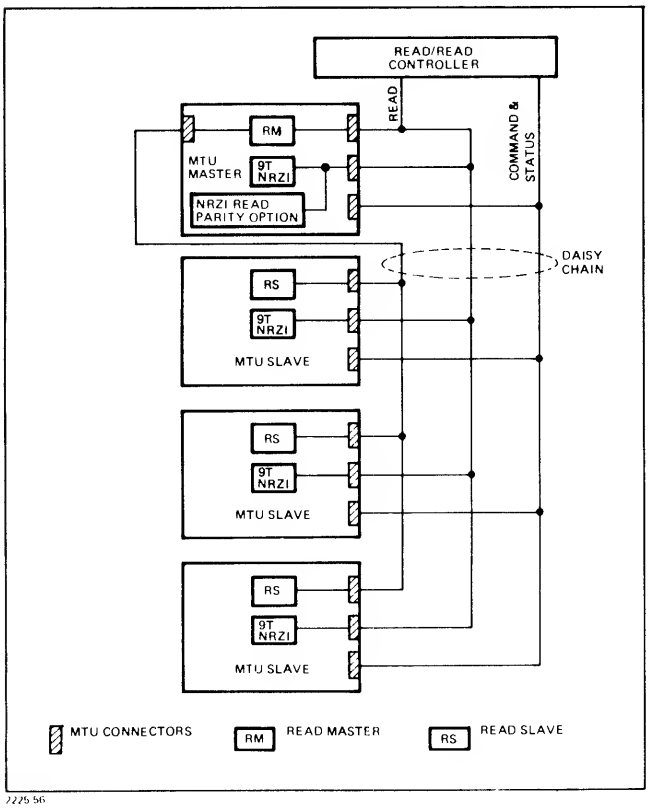


Figure 2-4. Dual Format (PE/NRZI), Master-to-Slave Configuration

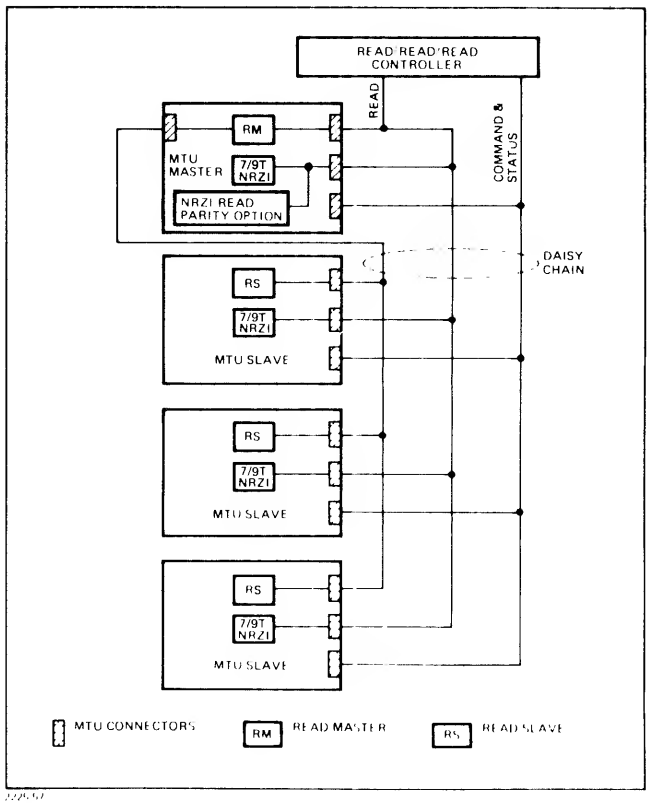


Figure 2-5. Multiple Format (PE/NRZI), Master-to-Slave Configuration

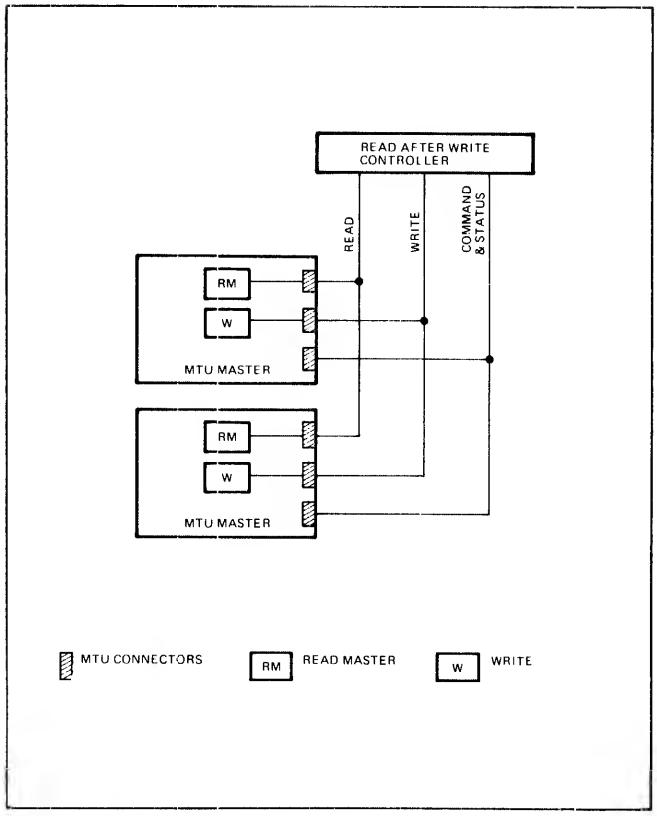


Figure 2-6. Read-After-Write, Master-to-Master Configuration

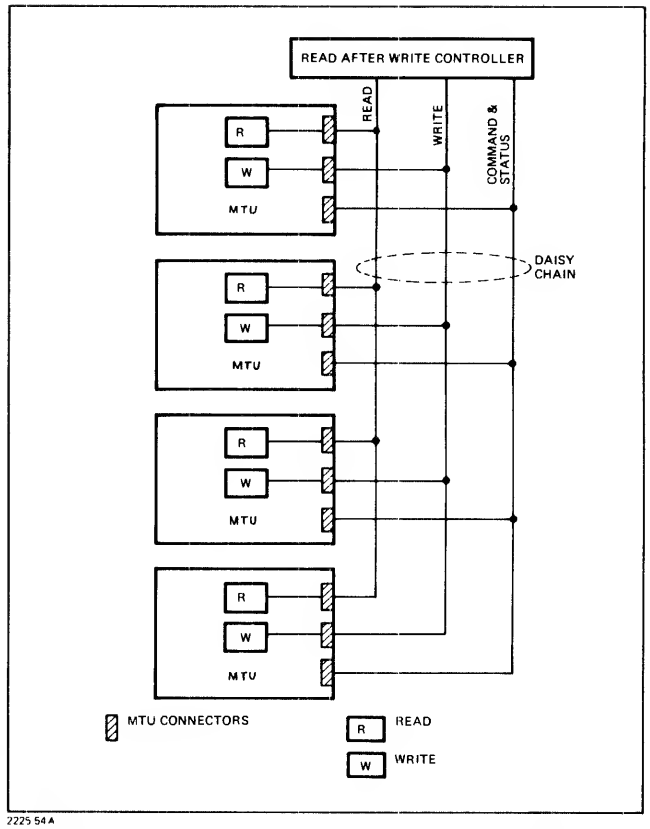


Figure 2-7. Read-After-Write, NRZI, Multiple Unit Configuration

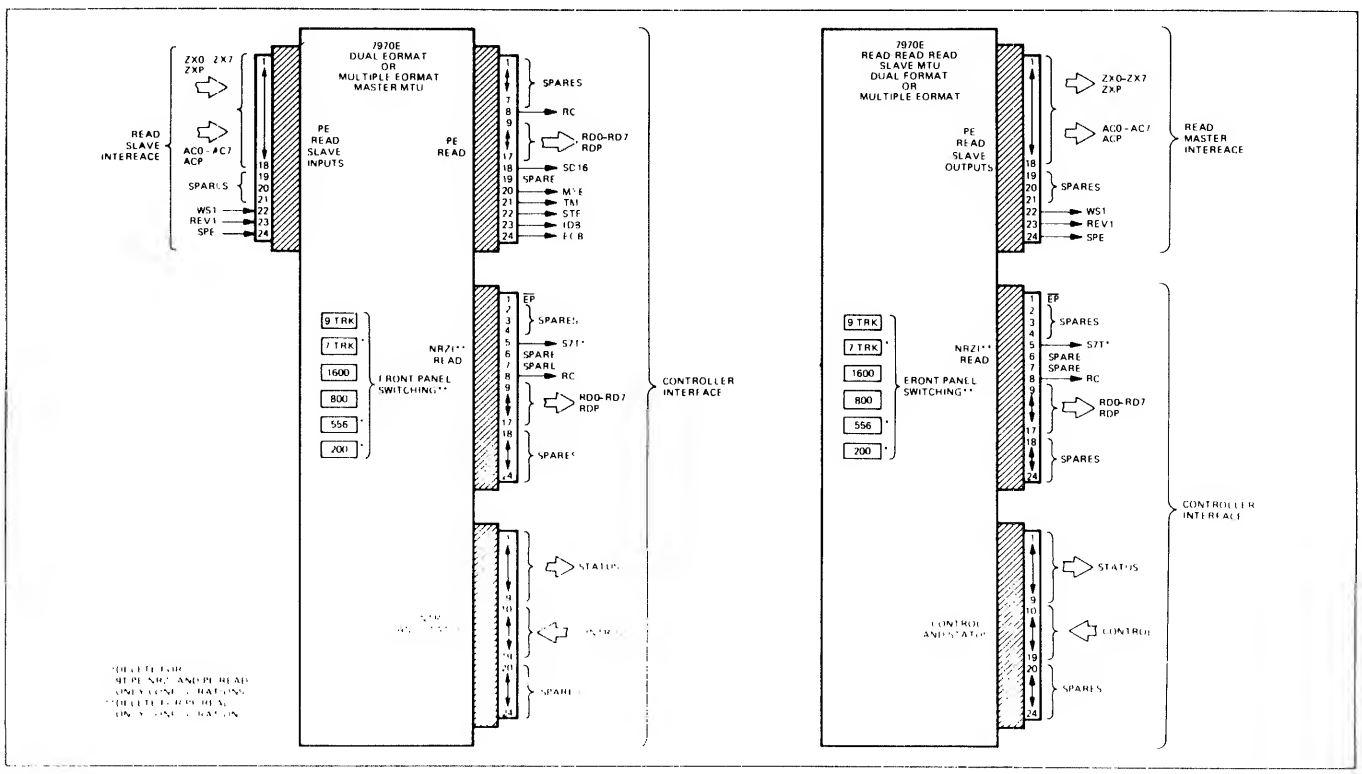


Figure 2-8. Multiple Format Configuration, Showing Connections

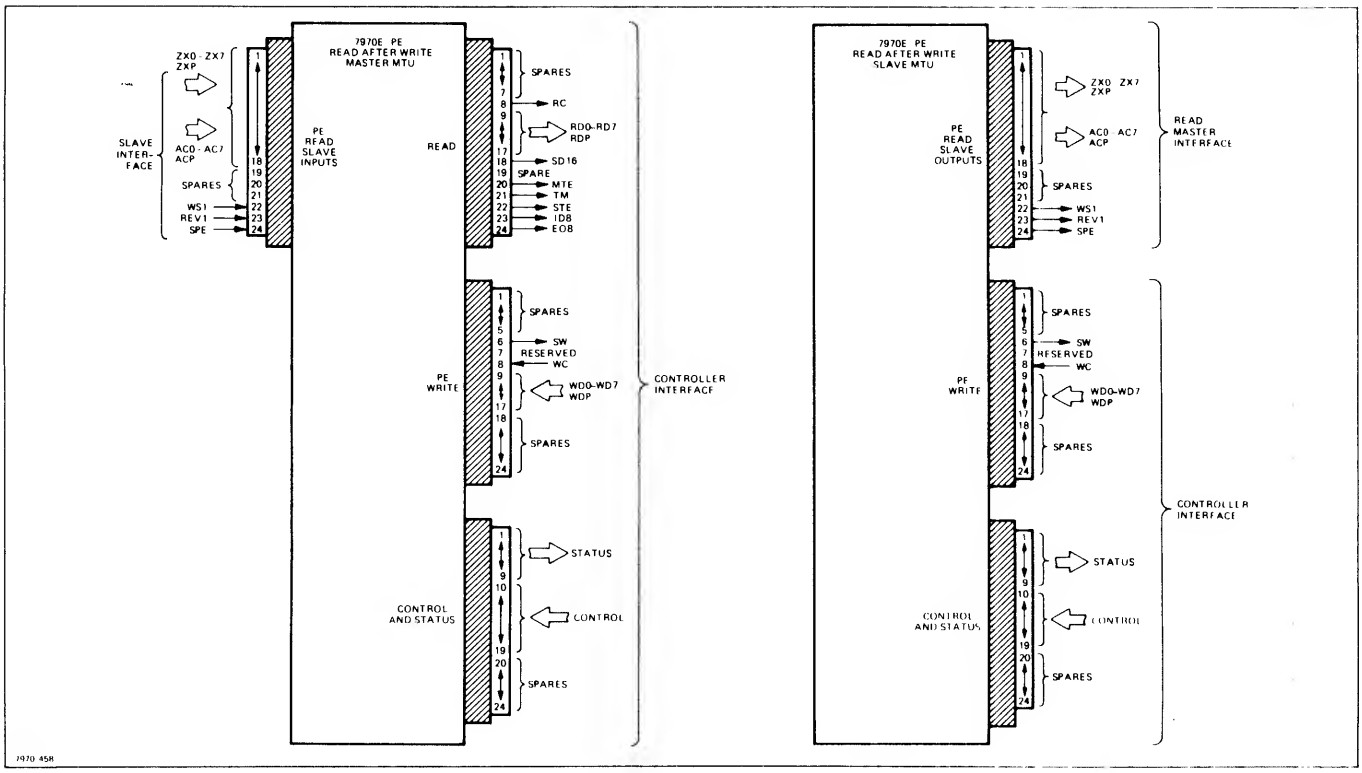


Figure 2-9. PE Read-After-Write Configuration, Showing Connections

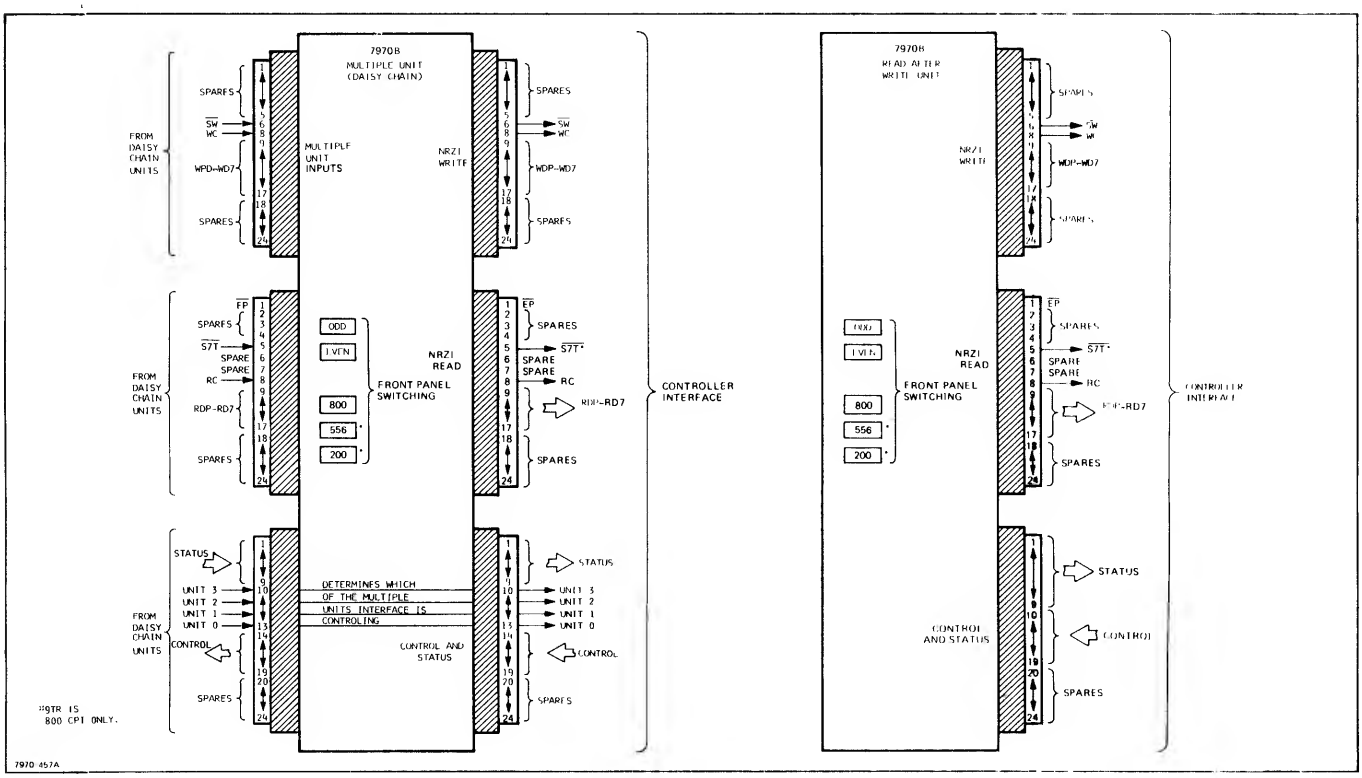


Figure 2-10. NRZI Read-After-Write Configuration, Showing Connections

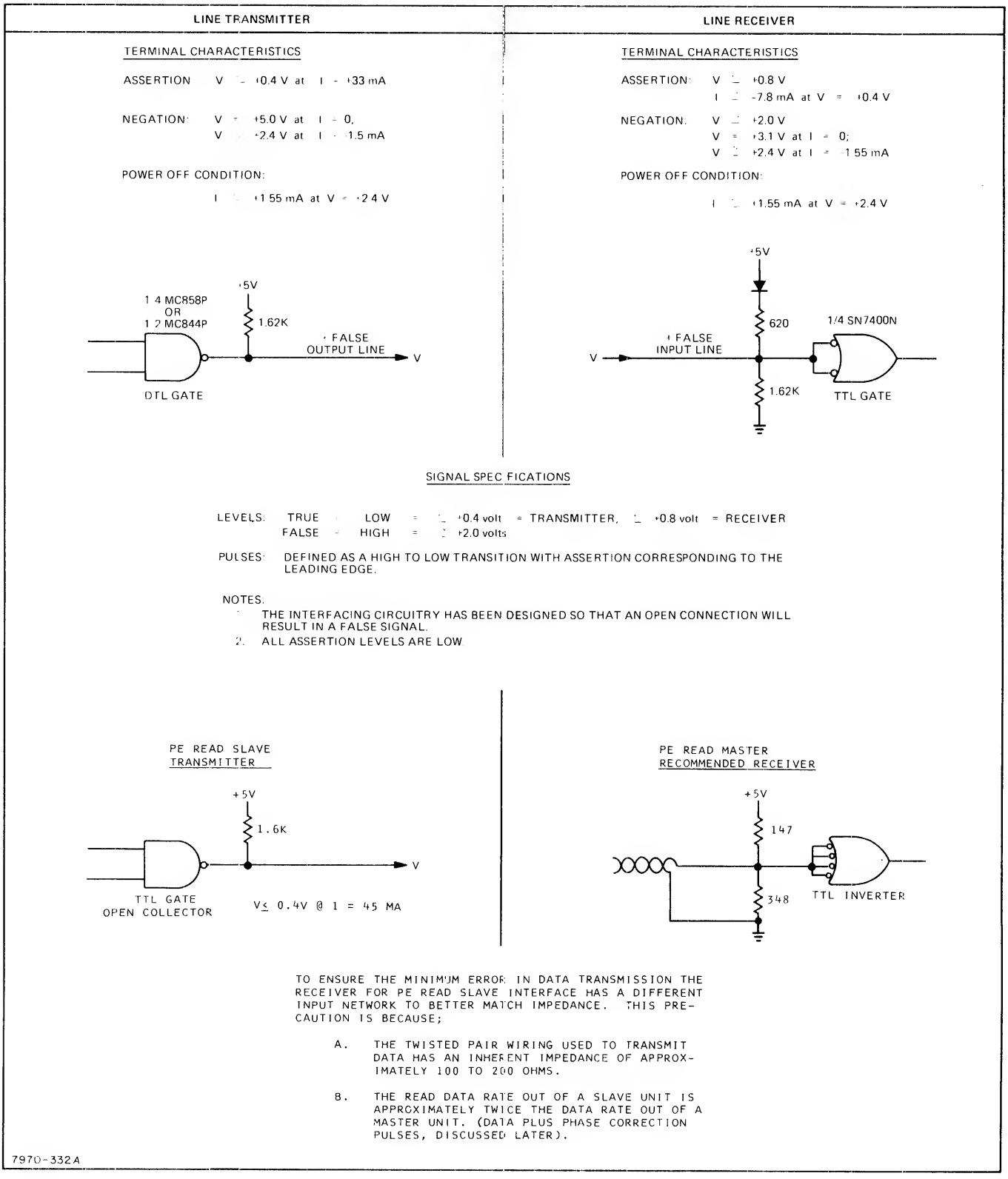


Figure 2-11. Parameters of I/O Line Transmitters and Receivers

2680-0107) and washers (part number 3050-0002) are installed in the holes provided in the casting. These screws prevent the casting from opening away from the housing.

b. Ensure that the inner carton is in good condition and that the liner (part number 9220-1660) is in position at the bottom of the inner carton. The slots in the liner allow the use of a shipping sling.

c. Place the unit into the inner carton with the reel cover facing up. Ensure that the casting weight is evenly distributed over the liner surface. If a shipping sling is used to lower the unit into the carton, be sure the webbing is located at the slots of the inner liner.

d. Place the plastic sheet over the unit to protect the window surface.

e. Place the top pad into position. If the unit is to be shipped without accessories, fill the remaining space with a filler carton or other similar filler. Do not fill this space with loose fill. Solid mass is required for adequate protection.

OPERATION

SECTION III

3-1. OPERATOR'S INFORMATION.

The operator will power-up the unit, install the tape supply reel, install the take-up reel, thread the tape, depress LOAD pushbutton and tension the tape, release LOAD pushbutton and allow tape to advance to the loadpoint, select the recording density (optional), position the unit select jumper on the control and status PCA as required, select the unit (optional), place the unit on-line, change supply reels as required, correct for a power failure, and manually rewind or unload tape as required.

Operator control of off-line functions is limited to the built-in manual controls, equipment options, and user interfaced provisions.

NOTE: Refer to Section I for control description.

3-2. MAGNETIC TAPE SELECTION.

Use computer grade tape, 0.5-inch wide and 1.5-mils thick.

3-3. CARE OF MAGNETIC TAPE.

Tape and reel should be handled carefully. Avoid unnecessary handling of tape to minimize tape contamination. Tape should be kept in the supplier's container when not in use, preferably stacked on end. Avoid exposure to strong magnetic fields or excessive heat (such as temporary storage in direct sunlight). When handling reels, support the reel at the hub flange to minimuze reel warpage.

3-4. TAPE STORAGE.

Store tape at operating room temperature (60^{o} to 80^{o} F, 15^{o} to 25^{o} C, 60% humidity) with reels on edge in the original boxes, book-shelf style. If reels are stored flat, avoid stacking. Run the tape occasionally to preserve its resistance to storage conditions. If tape is stored in an environment different from the using environment, allow 12 to 24 hours for the tape to reach environmental conditions before using.

3-5. INSTALLATION/REMOVAL OF WRITE ENABLE RING.

The write enable assembly is part of the write/read optional feature. Loaded tape reels from the tape supplier are fitted with a write enable ring. For write operation, the write enable ring is installed. For read operation, the write enable ring is removed. With the write enable ring removed, no inadvertent recording on the tape is possible. This, in essence, is a file protect feature.

3-6. INSTALLATION OF BOT AND EOT PHOTOSENSE TABS.

Install EOT (end-of-tape) and BOT (beginning-of-tape; also called loadpoint) tabs as indicated in figure 3-1. The ten-feet (Tab to end-of-tape) requirement is minimum. Handle tape with clean hands and avoid excessive handling in recording area. BOT and EOT tabs are installed by the tape supplier. However, if the tabs come loose of if new tabs are required because of tape breakage, they may be installed by the operator. Use IBM tabs (Hewlett-Packard part number 9162-0062 or equivalent. These tabs are made with a pressure-sensitive adhesive which is attached to the shiny (non-oxide) side of the tape.

3-7. TAPE REEL INSTALLATION.

Check supply reel before installing. Examine reel for warpage or accumulation of dust. Clean reel if dirty. Do not use damaged or warped reel. Open cover door and verify that transport area is clean. Pull supply hub flange, position on hub, press firmly and seat reel to hub. Keep even pressure on reel flange and seat quick disconnect lever.

3-8. TAPE THREADING PROCEDURE.

To thread tape proceed as follows:

a. Verify that tape path is clean.

b. Install tape supply and takeup reels.

c. Thread tape as shown in figure 3-2. (Verify that tape is installed between tape guide flanges).

d. Work two turns of tape on takeup reel.

e. Set power switch to ON.

f. Close cover door.

g. Press LOAD pushbutton and release. Motion control logic will initiate a loadpoint search (BOT tab). Tape will stop at load point and LOAD indicator will light.

NOTE: If, the tape unit is tensioned with the load point reflective tab under the photosense head, ready condition will not be set (ready is a result of loadpoint search being satisfied). With the drive in this condition, pressing the LOAD pushbutton gates Load Point and On-Line status signals to the interface without a Ready Status. However, On-Line and Load Point conditions will be indicated on the front panel. Ensure that the loadpoint reflective tab is not positioned under the photosense head when tape is tensioned. The tab should be on the supply reel or somewhere between the supply reel and the photosense head.

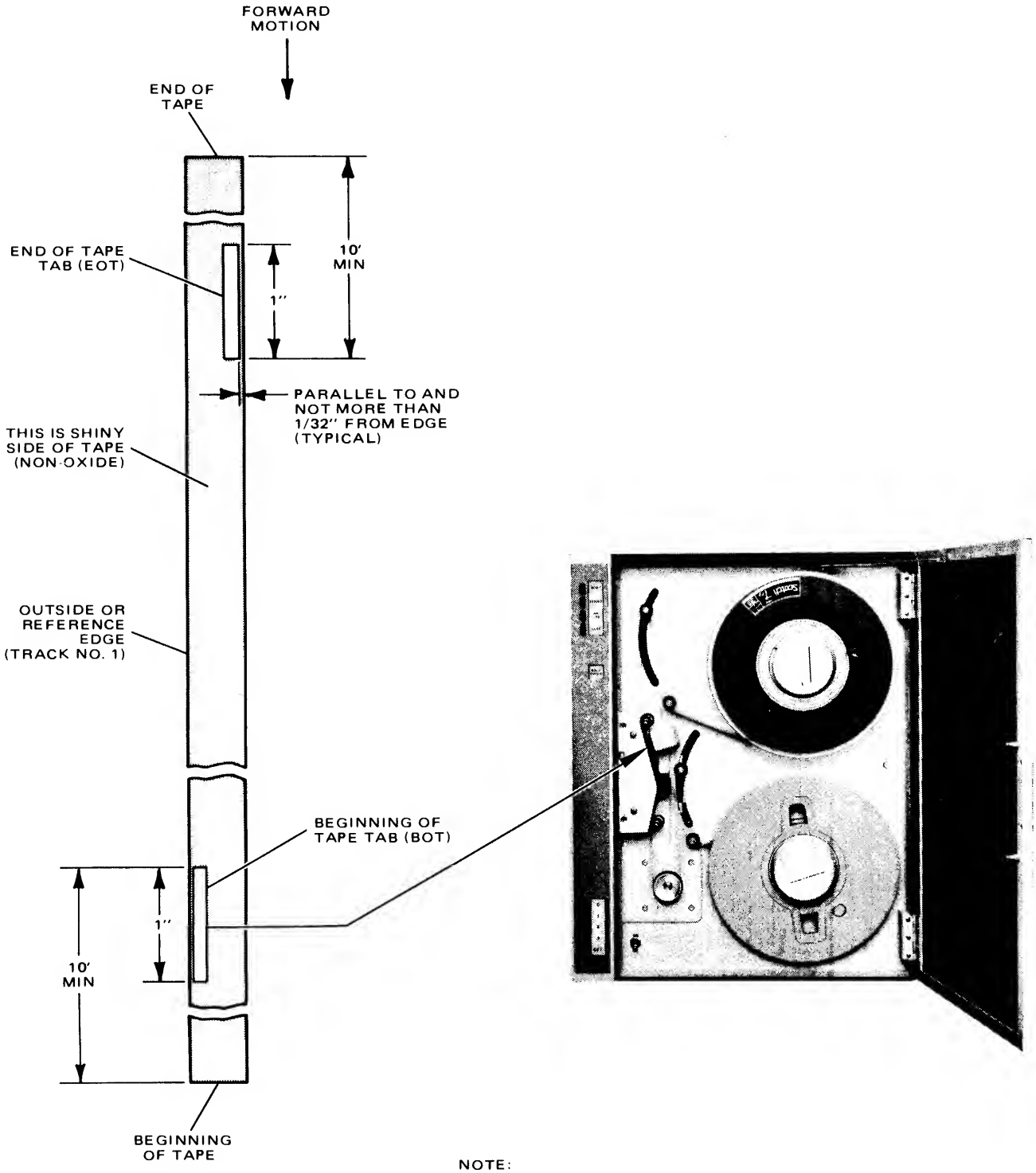
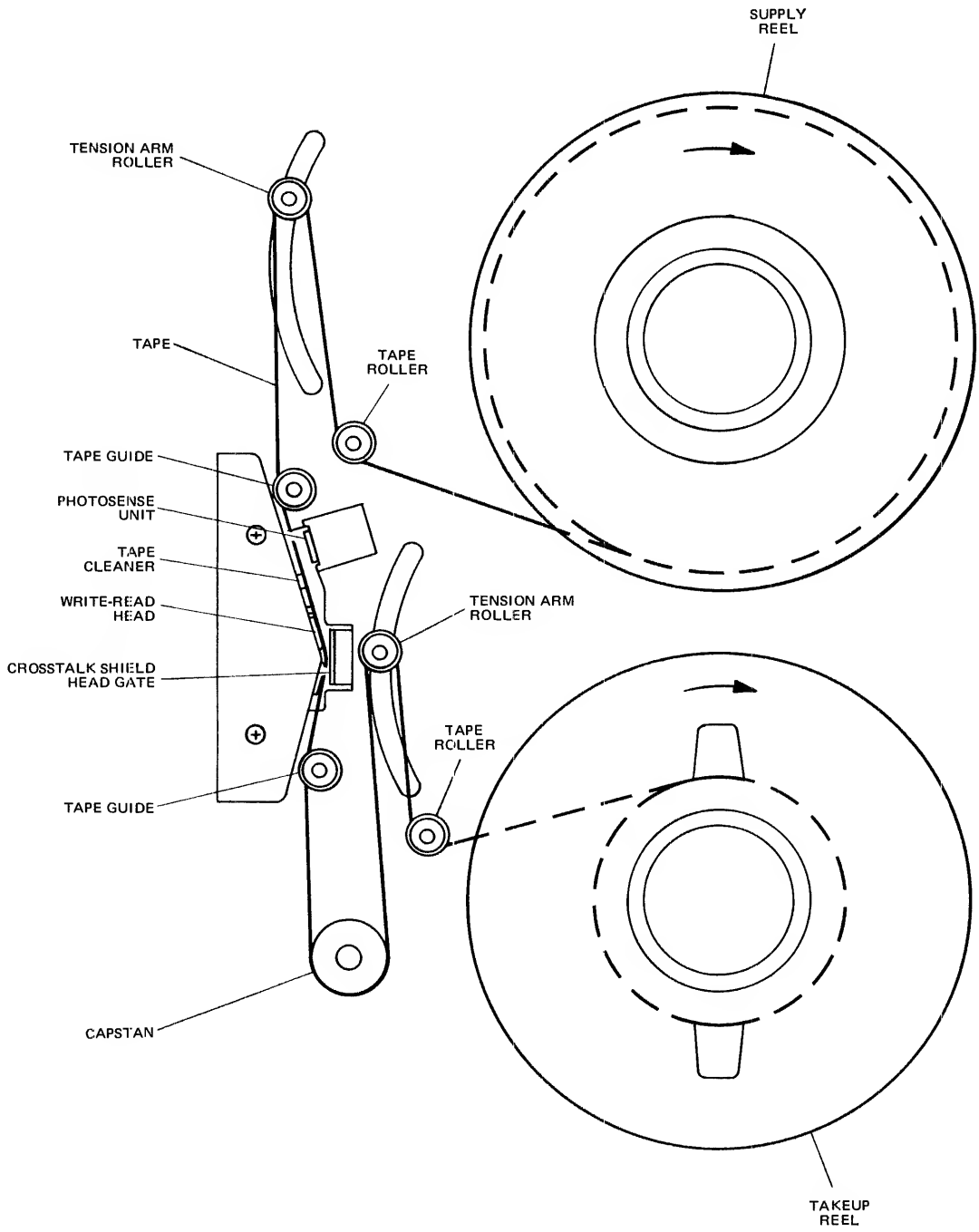


Figure 3-1. Installation of Photosense Tabs



7970-A-028

Figure 3-2. Tape Threading

3-9. CHECKOUT PROCEDURES.

The following performance checks may be used for incoming inspection or an an overall performance checkout after making adjustments or repairs. Off-line performance checks should be performed as soon as the unit is installed to determine that it is in proper working order. No test equipment is required. On-line performance checks will depend upon unit application. On-line refers to a unit that is physically connected to a controlling device, such as a computer, plotter, or key-to-tape system and is immediately addressable by the controller or requires a minimum amount of operator intervention such as pressing the on-line or address switches. On-line performance procedures check the tape motion response of the unit to processor commands, tape status output signals, and input-output data electronics. Where the unit is to be used for on-line application other than small computer peripheral application, the user should devise checks suitable to verify the special requirements.

3-10. OFF-LINE PERFORMANCE CHECKS.

3-11. MECHANICAL CHECK.

Perform mechanical check as follows:

a. Open and close cover door and verify that detents hold firmly.

b. Swing cover door open and verify that hinges are free and that the door stop bracket prevents the cover door opening more than approximately 105 degrees.

c. Press upper control panel pushbuttons and verify that the RESET, REWIND, ON-LINE, and LOAD pushbuttons press freely and lock in ON position.

d. Press density select, parity select, and unit select pushbuttons and verify that the mechanical interlocks are working properly. On each assembly each switch should lock ON when depressed and as the next switch is depressed the previous switch should release and return to OFF.

e. Release the transport latch and swing the main casting door out.

f. Slowly open and close main casting door and note that wire harnesses, wire cable, and ribbon cables fold properly.

g. Verify that all cable connectors are securely seated.

h. Verify that all motion and data cards are securely seated.

i. Verify that there is unobstructed airflow for instrument cooling.

j. Verify that unit select jumper on control and status PCA is connected to the proper pin. The proper pin connection is as follows:

(1) Tape units equipped with unit select option. Connect unit select jumper to pin labeled OFF.

(2) Tape units not equipped with unit select option. Connect unit select jumper to pin designating the desired unit number. (0, 1, 2, or 3).

k. Close and latch main casting door.

l. Open/close cover door and note that it rests snuggly against rubber seal.

3-12. MOTION CONTROL CHECKOUT PROCEDURE.

Perform the motion control checkout procedure as follows:

a. Check 115-230 Vac slide switch for proper line voltage selection, and connect ac power.

b. Verify that manual control switches located on the capstan servo PCA are in the OFF position (switch levers down).

c. Set power switch to ON. The following pushbutton indicators will illuminate: RESET, UNIT ADDRESS, and DENSITY SELECT.

d. Remove write enable ring from a reel of tape. Place reel on the supply hub (with BOT and EOT tabs attached). Reel should be seated firmly to the hub when the quick disconnect hub is latched.

e. Verify that empty reel on the takeup hub is properly seated.

f. Thread tape and verify that tape is inserted between tape guide flanges.

g. Press and hold LOAD pushbutton. Tape will move until tape tension arms are centered and proper tape tension is established.

h. Release LOAD pushbutton. Motion control logic initiates a loadpoint search. Tape will move forward at approximately 20 ips and will stop at loadpoint. LOAD indicator will illuminate.

i. Close cover door.

j. Press density select pushbuttons, one at a time, and note indicators. Pushbutton selected will illuminate then go dark when the next pushbutton is selected.

k. Press unit select pushbuttons: 0, 1, 2, 3, and OFF and note indicators. Leave the 0 unit selected. The 0 pushbutton indicator will illuminate and go dark when the 1 pushbutton is pressed, etc. Note that all unit select pushbuttons are dark, except OFF when OFF pushbutton is pressed.

l. Press ON-LINE pushbutton and release.

(1) ON-LINE pushbutton indicator will illuminate.

(2) The tape unit is now ready for processor control.

(3) The on-line condition negates the REWIND and LOAD pushbutton circuits.

(4) Press REWIND pushbutton; press LOAD pushbutton and observe transport response. No response should be observed.

(5) To remove the unit from on-line status, press RESET pushbutton.

(6) A substantial number of logic functions are initiated by the ON-LINE pushbutton. However, the following logic functions must occur before the unit is gated to status ready.

a. The On-Line signal is "and" gated with a Load Complete signal to generate a Ready signal.

b. The Ready signal is "and" gated with a Select-On-Line-Address (SOLA) signal to generate a Ready Status (SR) signal for the processor. (SR indicates that tape unit is selected, is on-line the initial loading sequence is complete, and the tape is not reqinding).

m. Press RESET pushbutton.

(1) ON-LINE indicator will go dark and RESET pushbutton will illuminate.

(2) Unit is now in off-line status. Manual controls are operative.

n. Check REWIND and capstan manual controls as follows:

(1) Open cover door and release transport main casting latch.

(2) Close cover door.

(3) Swing main casting door open.

(4) Set capstan servo FWD switch to ON (up). Observe that tape moves in forward direction.

(5) Set FWD switch to OFF. Observe that tape motion stops.

(6) Set capstan servo +160 (ips) switch to ON.

a. Observe that tape winds onto takeup reel at high speed.

b. Allow approximately 100 feet of tape to wind on takeup reel (seven or eight seconds).

c. Set +160 switch to OFF. Observe that tape motion stops.

(7) Set capstan servo REV switch to ON.

a. Observe that tape moves in reverse direction.

b. Set REV switch to OFF. Observe that tape movement stops.

(8) Press REWIND pushbutton (control panel). Observe that tape winds onto supply reel at high speed.

(9) Press RESET pushbutton.

a. Observe that tape movement stops.

b. REWIND pushbutton will go off.

c. RESET indicator will illuminate.

(10) Press REWIND pushbutton.

a. Observe that transport goes into fast rewind.

b. Close cover door.

c. Observe that RESET indicator is off.

d. Observe that REWIND indicator is illuminated.

e. Observe that tape winds past the loadpoint tab, stops, searches for the loadpoint, and comes to stop at loadpoint.

f. Observe that LOAD indicator illuminates.

(11) Hold REWIND pushbutton down until BOT tab passes photosense unit and then release pushbutton.

a. Observe that tape winds off the takeup reel.

b. Observe that REWIND pushbutton goes dark.

c. The following pushbutton indicators will illuminate: RESET, DENSITY SELECT, and ADDRESS SELECT.

o. Remove supply reel and install write enable ring.

p. Install supply reel. Observe that WRITE ENABLE indicator is illuminated.

q. Return unit to original configuration.

3-13. OPERATION.

The tape unit is designed for processor (computer) controlled operation. However, manual controls are provided to bring the unit to on-line status, to restart after a power failure, and as a service aid during repair or checkout. The controls that the operator will normally use are located on the control panel.

NOTE: In multiple unit installations and when reading, do not power down more than one unit at a time. If power is removed from more than one unit circuit loading may cause intermittent operation.

3-14. ON-LINE READ OPERATION.

To operate the unit in read mode, proceed as follows:

a. Remove write enable ring from supply reel.

b. Install supply reel.

c. Thread tape and place tape at loadpoint.

d. If unit is equipped with a density select option, press density selection.

e. If unit is equipped with a parity select option (multiple format units) press parity selection.

f. If unit is equipped with a unit select option, press address pushbutton. If not, connect unit select jumper on control and status PCA to proper pin for tape unit selection by the controller.

g. Press ON-LINE pushbutton. Unit is now in ready status under processor control.

h. To stop unit, press RESET.

i. Press ON-LINE to place unit under control of processor.

j. Press unit select OFF pushbutton to remove unit from processor control without disturbing unit logic. To place unit under processor control again, press unit select pushbutton.

3-15. ON-LINE WRITE OPERATION.

To operate the unit in write mode, proceed as follows:

a. Install write enable ring to supply reel.

b. The rest of this procedure is identical to the read only operation. Refer to paragraph 3-14 (steps "b" through "j").

3-16. REWIND.

High-speed rewind can be initiated during any tape function by pressing RESET and then pressing REWIND. To stop rewind at any tape position, press RESET. To resume rewind, press REWIND. Fast rewind will continue until the loadpoint tab is sensed and passed. Unit logic will automatically go into loadpoint search and stop at loadpoint.

3-17. RESTART AFTER POWER FAILURE.

After a power failure during a read or write operation, the unit will be off-line. To resume interrupted function, proceed as follows:

a. Open cover door.

b. Verify that tape is on guides.

c. Press LOAD.

d. Close cover door.

e. Press RESET.

f. Press ON-LINE.

3-18. REV, FWD, AND +160 CAPSTAN SERVO TOGGLE SWITCHES.

To use the REV (reverse), FWD (forward), and +160 (high-speed forward 160 ips) for service switches proceed as follows:

NOTE: These switches are for service only.

a. Open cover door.

b. Install tape supply reel.

c. Thread tape.

d. Set power switch to ON.

e. Tension tape. Depress load pushbutton.

f. Release transport latch.

g. Close cover door and swing main casting door open.

h. Operate service switches as desired.

i. Leave all switches in OFF position before assuming normal operation.

THEORY OF OPERATION

SECTION IV

4-1. INTRODUCTION.

This section provides an overall functional description of the tape unit circuitry at a block diagram level. Where necessary because of extensive changes or unusual circuitry a more detailed circuit analysis is given.

4-2. N.R.Z.I. AND P.E. CODES AND TAPE FORMATS.

Non Return to Zero Inverted (NRZI) and Phase Encoded (PE) are the two methods of reading and writing data used in 7970B and 7970E tape drives. Respectively the 7970B is NRZI only, and the 7970E can be PE (standard) or PE and NRZI (multiformat). The 7970E multiformat tape drive is read only, and NRZI read electronics are installed in place of the PE write electronics.

NRZI recording is accomplished by a change in flux to write a "ONE" and no change in flux to write a "ZERO". One channel is graphically represented as shown in figure 4-1.

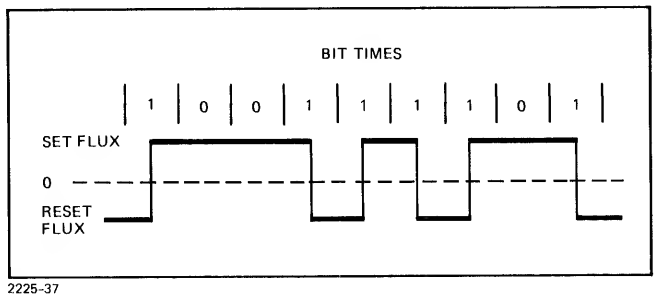


Figure 4-1. NRZI Code Flux Pattern

Since no flux change occurs when a zero is written and we use the output from the tape to generate the read clock, it is necessary to write a "one" in at least one channel each bit time. In 9 track tape drives odd parity is used for lateral error checking. Thus, if the tape unit is provided with an all zeros byte (8 bits of data) the parity circuits, either on the interface or the optional write parity card, will generate a "one" bit in the ninth channel. This parity bit is used to generate the clock in this case. In 7 track even parity, an all zeros byte is not allowed.

NOTE: Seven track tape drives write ASCII code. A space in ASCII code is coded octal 40. (40_8 = 100 000).

Parity is discussed in more detail in a later paragraph.

NRZI read is discussed in detail in the read data circuits; however, as in recording, a flux reversal indicates a "ONE" and no reversal indicates a "ZERO".

To accomplish PE recording, a change of flux is required to write either a "ONE" or a "ZERO". A change of flux in one given direction writes a "ONE" and a change

in the other direction writes a "ZERO". (Write head driver goes from set to reset = ONE, driver goes from reset to set = ZERO). Since the polarity (phase) of flux determines whether we write a one or a zero, we must insert a correction signal (phase correction) between like data bits to establish the correct reference state (set or reset) for the next bit to be written. See figure 4-2, one channel, typical.

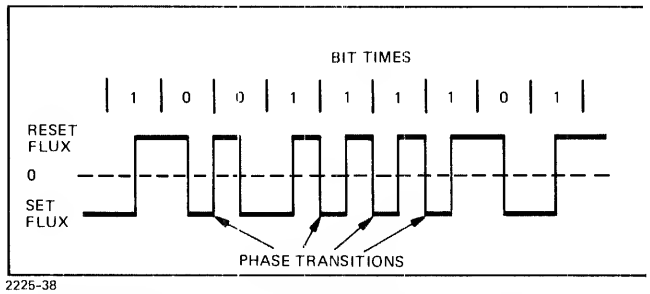


Figure 4-2. PE Code Flux Pattern

By monitoring the present state and the next data bit to be written, the interface or the optional write data formatter will determine if a phase correction is required. The tape drive write electronics contains no look ahead electronics.

NRZI Tape Format. 9 track NRZI tape information consists of three types of information blocks; Density Identification area, Data Blocks, and Tape (file) Mark, see figure 4-3. The density identification area is fully saturated in the erase direction (blank). It begins slightly ahead of the BOT marker and ends slightly after the BOT marker (1.3 inches minimum length). The first data block follows the initial gap (3.0 inches minimum) and the data block is 18 to 2048 characters in length. The data is immediately available at the end of a gap and the end of data is noted by no data in any channel for more than two bit times. Four byte spaces after the last data bit a byte is written (CRCC), cyclic redundancy check character that is part of the error correction. After four more bit times the longitudinal redundancy character check (LRCC) is written. Seven track is basically the same as the nine track explanation except there is no CRCC byte. The tape mark is a byte with a '1' written in channels 3, 6, 7.

4-3. PE TAPE FORMAT.

PE tape information consists of three types of information blocks; identification burst blocks, data blocks, and tape (file) mark blocks. (Figure 4-4). The identification burst (IDB) consists of flux reversals in the parity channel only. It begins slightly ahead of the beginning of tape (BOT) marker and ends slightly after the BOT marker. The first data block follows the IDB after a gap of at least 3 inches. A data block consists of three parts or sections; a preamble, data section, and a postamble. The preamble consists of 41 bytes; 40 logic 0 bits in every channel followed by one logic 1 bit in every channel. The data section normally consists of 18 to 2048 bytes. However, it can be of any desired length. The postamble is a 41 byte section which consists of one logic 1 in every channel followed by 40

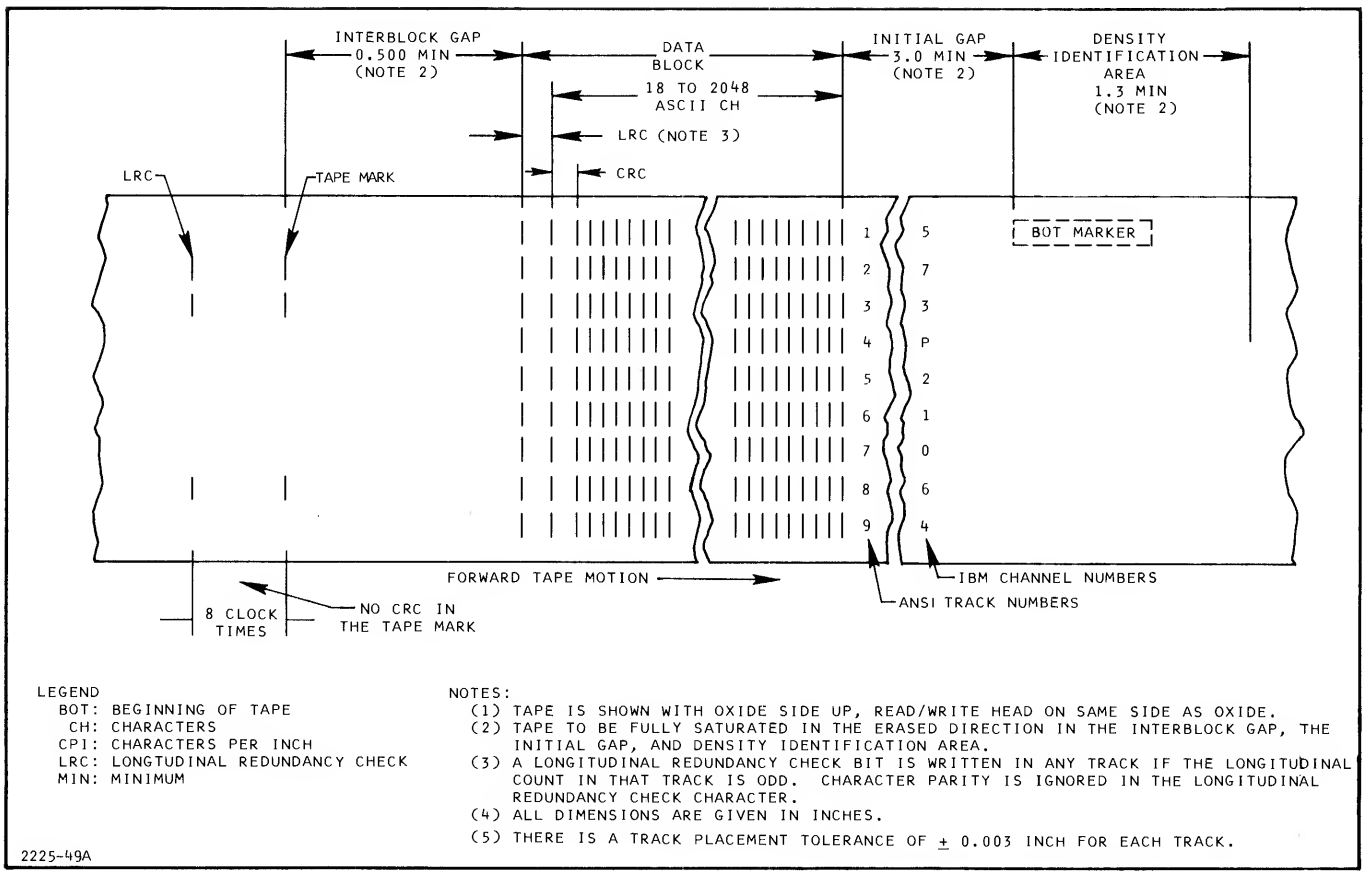


Figure 4-3. NRZI Tape Format

logic 0's. Data blocks are separated by inter-block gaps greater than 0.5 inch long. Tape marks are used to separate data blocks into groups or files. A tape mark consists of from 64 to 256 flux reversals in channels two, six, and seven. (IBM channel numbers), or channels P, zero, and five. However, at the same time channels one, three and four (IBM) must be without flux reversals.

4-4. TAPE DRIVE OVERALL FUNCTIONAL DESCRIPTION.

At initial power-on, the capstan motor is open, and the reel servo motors are shorted. When the LOAD switch is pressed, the capstan motor and reel motor circuits are completed. When tape tension is established, the tension arms swing away from the tension limit switches. With tape tensioned, the capstan and reel motor returns are maintained. When the LOAD switch is released, the control and status circuits initiate a load point search. During load point search, the reel servo circuit operates in the synchronous range (normal) and the capstan servo pulls tape forward at approximately 20 ips.

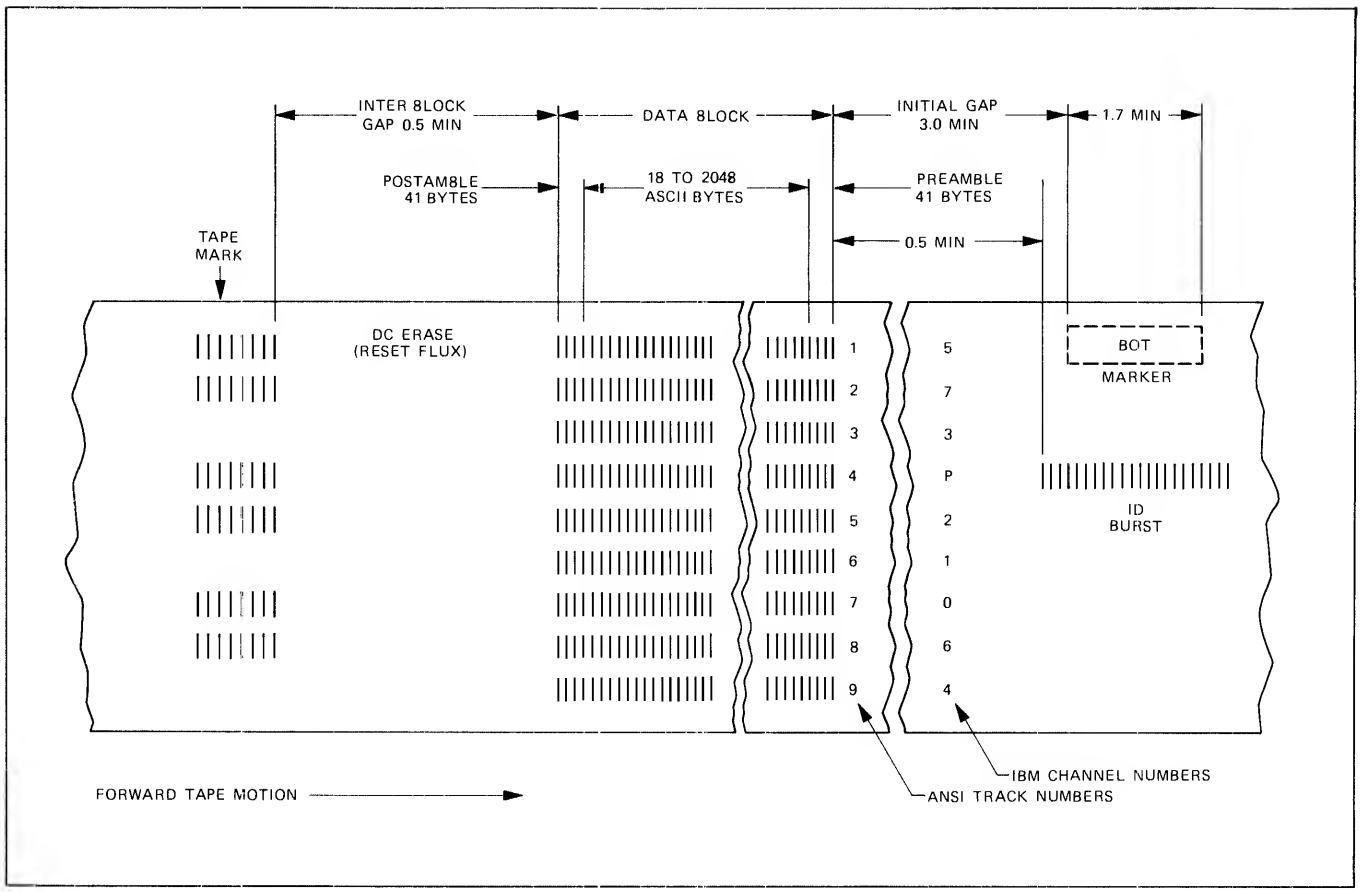


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Figure 4-4. PE Tape Format

When the load point tab is detected by the photosense assembly, the control and status circuits terminate the load point search, and tape motion stops. The control and status circuits provide a load point status to the interface, and the front panel LOAD indicator illuminates.

Pressing the ON-LINE switch establishes interface control of the tape unit. Except for RESET, the front panel controls now have no control of the tape unit. Pressing RESET releases the interface control and allows front panel control of the tape unit.

When the tape unit is under interface control and data is being processed, the tape unit pulls tape at synchronous speed as required and tension is maintained. When the end-of-tape tab is detected, the control and status circuits provide the interface with an end-of-tape (EOT) status.

A rewind command generated by the interface will initiate the rewind sequence. The control and status circuits place the capstan servo circuits in a highspeed reverse mode and switch the reel servo feedback circuits for high gain. The capstan rewinds tape at 160 ips and the reel servo operates in the high gain region. When the

trailing edge of the beginning-of-tape (BOT) tab is detected, the control and status circuits terminate the rewind mode, and after a one-second delay, establish a load point search.

Pressing RESET releases the tape unit from interface control. Pressing RE-WIND in this condition (load point) rewinds the remainder of the tape onto the supply reel. When the tape is depleted on the take-up reel, the tension arms contact the tension arm limit switches, the capstan motor circuit is broken and the reel motors are shorted. This provides dynamic braking of the reel motors.

When the tape unit (write/read units only) are loaded with a reel of tape equipped with a write enable ring, the write enable assembly provides +12 volts (+12 WE) to the write data circuits. The +12 WE provides write current for the write head drivers and the erase head driver. Tape unit motion status signals and interface commands are processed by the write control circuits to control the write data circuits. The write control circuits also provide a Write Latch status signal which is used to switch the read threshold level.

Information to be written onto tape is provided by the interface and processed by the tape unit write data circuits. When the unit write condition is first established, the write control circuits ensure that the write head drivers are in a reset state (inter-record gap flux) and tape is saturated in the same polarity as the erase head.

After all the characters of a data block have been written, WRS from the interface causes an additional flux reversal to be generated if an off number of bits was written in the channel. All write head drivers are therefore left in a reset state.

When reading from magnetic tape, an analog signal is generated and the coding of information on the tape is such that every byte contains a flux reversal in at least one of the tracks. All bits that make up a character byte may not arrive at the head at the same time. This is known as (skew). The read data circuits detect the flux transitions in each track, correct for skew and produce a parallel digit output with all bits of the character byte presented simultaneously.

The NRZI tape drives have an adjustment in each channel to delay any individual channels' bit for alignment purposes. Recovery of the data is accomplished by generating a fixed-time window or character gate. Starting with the first detected flux reversal, all remaining bits must arrive during the character gate. At the end of the character gate time, a read strobe pulse samples the contents of all input registers for the next data byte.

In the PE tape drives each channel decoder has its own window generator which sets up circuitry to strip out phase correction signals from data. The window time allows data bits to be shifted into each channel's four-bit skew buffers. Presence of data in the skew buffer indicates data is ready on this channel. The four bit skew buffers give the unit time to sample all channels for data and not have to worry about skew. As a result the PE read units have no mechanical means of deskew. The skew buffer and window logic is discussed in more detail later.

4-5. TRANSFORMER ASSEMBLY AND POWER DISTRIBUTION ASSEMBLY.

All tape units contain similar power supplies, which consist of the transformer assembly, power distribution assembly, and power regulator assembly. Minor part differences on each assembly occur between units due to a difference in power requirements; however, circuit operation is identical in all units. A tape unit operates from either a 115 or 230 Vac power source with full-wave rectification occurring in the transformer assembly. The transformer assembly delivers +59, -59, +24, -24, and +13 unregulated dc voltage to the power distribution assembly and power regulator assembly. The +13 Vdc input is used as a source for a +5 Vdc regulated output, while the +24 Vdc and -24 Vdc inputs are also used to supply +20 Vdc (nominal) and -20 Vdc (nominal) to the capstan servo assembly and the reel servo assembly. The +59 and -59 Vdc provide +40 Vdc (nominal) and -40 Vdc (nominal) to the reel motor servo assemlby during high speed forward or reverse operation. Switching from 20 Vdc to 40 Vdc is accomplished on the power regulator assembly.

4-6. Transformer Assembly. The transformer assembly contains a power transformer, three bridge rectifiers, filter capacitors, and bleeder resistors. (Refer to parts and diagram manual, part no. 07970-90886). The primary circuit of the power supply transformer includes a switch that allows selection of 115 or 230 Vac operation, a power on-off switch, and a line filter/power connector. When 115 Vac power is selected, the two primary windings of the power transformer are in parallel and fuse F1 provides overload protection. When 230 Vac power is selected the two primary windings of the power transformer are in series, and fuse F2 is placed in series with the primary winding to provide overload protection.

4-7. Power Distribution Assembly. The power distribution assembly (See figure 1-3) contains secondary fuses and connectors for power distribution. The assembly also contains a printed-circuit connector for the power regulator printed-circuit assembly. Silicon diodes in the ±20 volt circuits and the ±12 volt distribution circuits provide circuit protection.

Unregulated power from the power supply is distributed to the power regulator printed-circuit assembly and to heatsink-mounted power transisitors. Unregulated ±40 volts (57.5 volts nominal) from the power supply is routed through heatsink-mounted resistors to the power regulator printed-circuit assembly. Regulated power (+5V, +12V, and -12V) from the regulator-controlled transistors (heatsink-mounted) are distributed to the transport circuits and data circuits by the power distribution printed-circuit assembly.

Unregulated ±20 volts (22.5 volts nominal) from the power supply is provided for the reel servo circuit. The switching circuit on the Power Regulator PCA causes the ±20/40 volt lines to switch from 22'5 volts dc to 57.5 volts dc. Diodes CR3 and CR4 (power distribution PCA) are protection in the event a short circuit takes place between the plus and minus 22.5 volt DC lines (on the reel servo for instance). They prevent any possibility of reversal of the +5, +12, and -12 volt DC polarity caused by the type of short mentioned.

4-8. Power Regulator PCA. The power regulator printed-circuit assembly contains a +12 volt regulator circuit, a -12 volt regulator circuit, and a +5 volt regulator circuit. (See figure 4-5). The power regulator printed-circuit assembly also contains a reel servo voltage switching circuit and a delay circuit. These circuits and related circuits are described as follows:

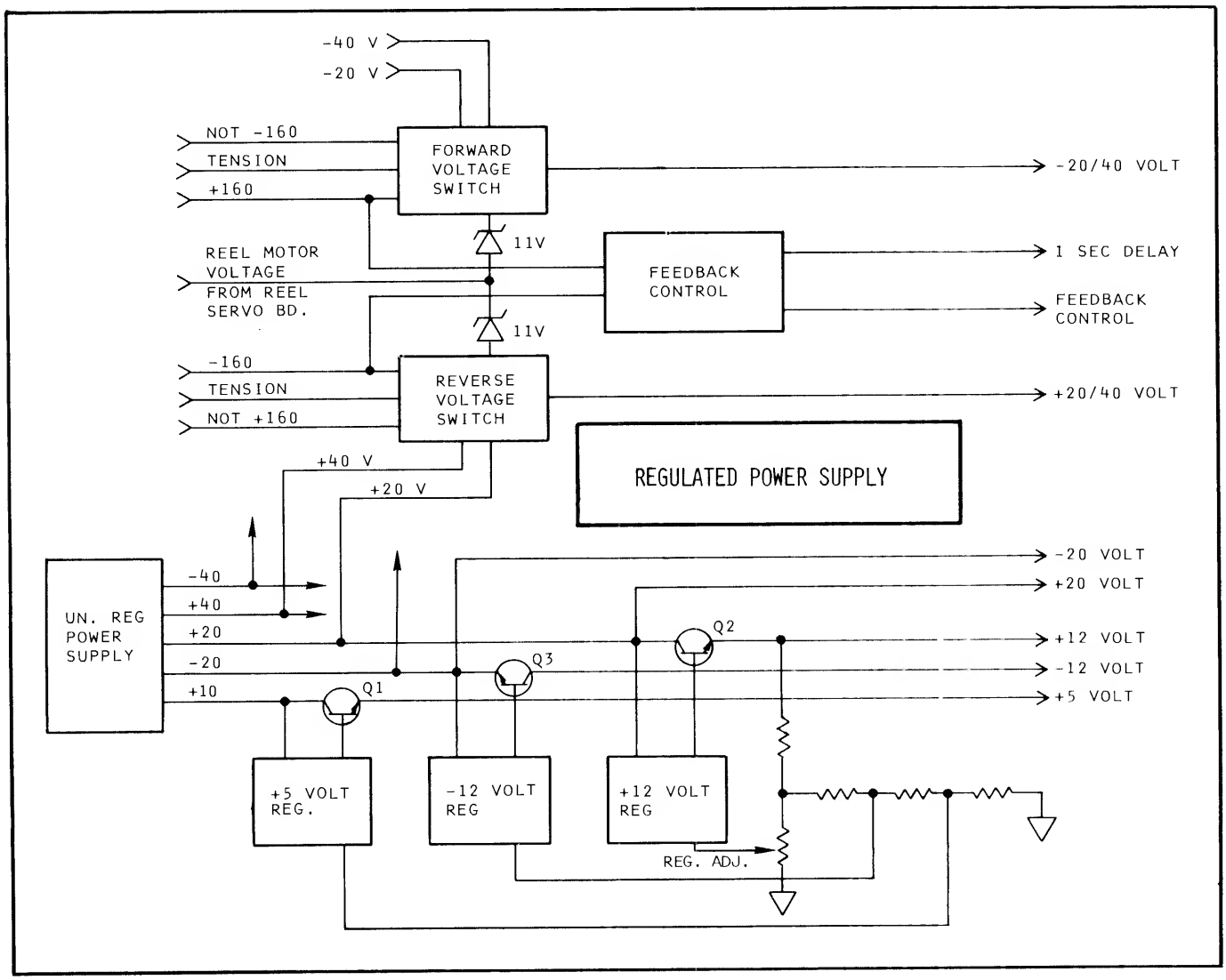


Figure 4-5. Regulated Power Supply Block Diagram

4-9. +12 Volt Regulator. The +12 volt regulator uses an integrated circuit voltage regulator with an internal temperature compensated voltage reference.

Regulation is obtained by dividing the output voltage (R3, R4, and R5) and comparing the divided voltage with the internal reference. The output voltage of the +12 volt regulator is adjustable by variable resistor R4. Series regulator transistor Q2 (located on a heatsink external to the regulator) is protected by current limiting. The current foldback knee is set to approximately 2.8 amperes by R1 and R2. Short circuit current is set to approximately 1.3 amperes by R7 and R8 (located on the heatsink external to the regulator).

4-10. -12 Volt Regulator. The -12 volt reguator uses an integrated circuit voltage regulator. The reference for the -12 volt regulator is derived from the regulated +12 volt source. Current limiting of the -12 volt regulator is set at 1.2 amperes as determined by R9. Diode CR7 limits the output voltage to -14.7 volts in the event that the +12 volt reference is lost.

4-11. +5 Volt Regulator. The +5 volt regulator uses an itegrated circuit voltage regulator. The reference for the +5 volt regulator is the +12 volt regulator output using R23, R25, and R26. Current limit of the +5 volt regulator is approximately 4.0 amperes (8.0 amperes on 7970E) controlled by current sense resistor R6, located external of the regulator on a heatsink. In the event of an overvoltage condition, silicon controlled rectifier CR1 conducts and shorts the +5 volt supply. The 4 ampere short circuit current will blow fuse F5 which is in series with the +10 volt unregulated supply.

4-12. Voltage Switching Circuit. When the high speed logic inputs from the reel servo PCA are present, the output of Q18 switches the reel servo amplifier to high gain. As the drive signal at the output of the servo amplifier reaches a sufficient amplitude to break down CR4 and CR6 (REV or FWD) the plus or minus 20VDC is switched to plus or minus 40VDC. (plus = Reverse, minus = forward).

4-13. TRANSPORT.

Most of the transport circuits are contained on the capstan and reel servo PCA's.

4-14. Capstan Servo Circuits. The capstan servo circuits control the speed and direction of tape motion across the magnetic head assembly. The capstan servo consists of a capstan motor/tachometer and a capstan servo printed-circuit assembly. The servo circuit employs current and velocity feedback. The velocity feedback is provided by the magnetic moving coil tachometer attached to the capstan motor shaft. Current feedback is provided by a pair of sensing resistors in the capstan motor return circuit. Figure 4-6 is a block diagram of the capstan servo circuit. The capstan is the only device on the 7970E transport used for driving tape. Therefore, the capstan drive servo amplifier must be capable of moving tape at 5 different speeds; forward/reverse synchronous (normal speed), high speed forward/reverse (160 IPS) and load point search speed (20 IPS). Capstan servo command lines enter the servo board from the control and status board and are applied to one of five reference voltage sources.

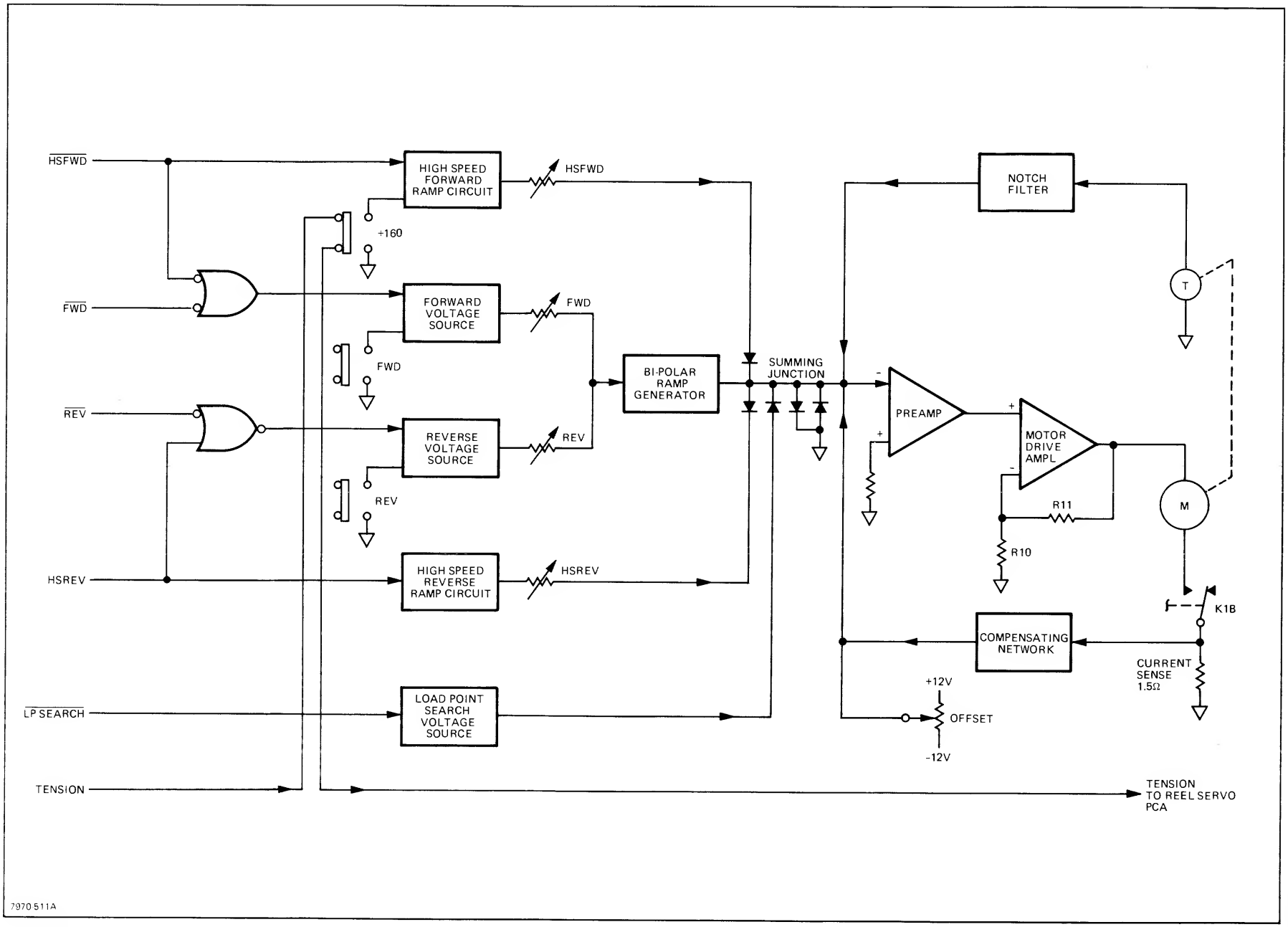


Figure 4-6. Capstan Servo Loop, Block Diagram

Output from the high speed forward and high speed reverse voltage sources is adjustable and provide an input to a summing function. Output from the forward and reverse synchronous sources is adjustable and provide input to the bi-polar ramp generator. The slope of the ramp generator output is adjustable to permit changing the start-stop distance; and provides synchronous speed input to the summing junction. The load point search voltage source provides a non-adjustable 20 IPS drive source to the summing junction. An offset potentiometer is used to compensate for any component leakage and to "zero" the summing junction. The summing junction provides input to a preamp which simultaneously feeds two complimentary power amplifiers. The appropriate power amplifier drives the capstan motor causing tape motion. Velocity feedback voltage relative to capstan speed is developed by a tachometer and is presented to the summing junction along with motor current feedback which is developed across the current sense resistor. These two feedback voltages oppose the applied drive voltage to maintain a uniform tape speed. A connector (J-6) is placed in one of 6 positions tc allow correct operation of the capstan servo motor assembly. Damage to the PCA or capstan motor may result if J-6 is missing or incorrectly installed.

NOTE: Use the parts and diagrams manual as an aid in the following explanation.

The capstan motor is driven by current generated by integrating preamplifier U4 and motordrive amplifiers Q1 through Q6 on the capstan servo PCA. The direction and speed of the tape motion is controlled by the polarity and magnitude, respectively, of the current supplies to the motor by motor-drive amplifiers Q1 through Q6. Transistors Q2, Q4, and Q6 supply current for forward tape motion and Q1, Q3, and Q5 supply current for reverse tape motion.

NOTE: The following paragraphs describe operation of a single speed capstan servo PCA. The last paragraph of the capstan servo discussion describes the differences between a dual speed and single speed capstan servo PCA.

The polarity and magnitude of the current supplied to the capstan motor (by the single-speed capstan servo PCA) is determined by the polarity and magnitude of the algebraic sum of currents at the input (pin 2) to integrating preamplifier U4. This current-summing junction has four current sources; the bipolar ramp generator (U2, U3 and R66), the high-speed forward ramp circuit (U1B, Q8, C25, and Q9), the high-speed reverse ramp circuit (Q13, Q10, C26, and Q11), and the load point search voltage source (Q12). Clipping diodes CR17 and CR18 limit the input voltage to preamplifier U4 to a relatively low value.

The bipolar ramp generator consists of high-gain amplifier U2 and integrating amplifier U3. It converts the step voltage inputs from the forward and reverse voltage sources to positive-going (forward) and negative-going (reverse) ramp voltages. A clipping network (CR7 through CR11) limits the voltage at the point common to R39 and R40 to a maximum of approximately 7.5 volts, regardless of its polarity. Amplifier U2 is a saturating amplifier (with a voltage gain of approximately 100) with no phase inversion. Integrator U3 inverts its input, converting a positive step input to a negative -going ramp and a negative step input to a positive-going ramp. Negative feedback from the output of U3 to the input of U2 through R66, combines U2 and U3 into a single ramp generator. The feedback through R66 helps linearize the ramp voltage output supplied to the summing junction. The slope of the ramp is con-

troled primarily by C28, R40, R41, and R43. Adjustment of the ramp slope is enabled by variable resistor R42.

With both the HSFWD and FWD signals inactive (high) and both the +160 and FWD switches in the off position, both inputs to U1D are high, Q7 is on, and zero volts is present at the junction of CR5, CR6, and R34. This leaves the voltage at the input to the bipolar ramp generator dependent on the input voltage supplied by the reverse voltage source.

When either the HSFWD or FWD signal is active (low) or one of the two switches is closed, Q7 is off. With Q7 off, a voltage of -6.2 volts is present at the junction of CR5, CR6, and R34. Assuming the output of the reverse voltage source (at the point common to CR1, CR2, and R28) is at zero volts, this applies a negative voltage to the bipolar ramp generator. This results in forward tape motion at synchronous speed. Variable resistor R34 adjusts the ramp generator input voltage to produce the desired forward synchronous tape speed.

With both the HSREV and REV signals inactive (low and high, respectively) and the REV switch in the open position, U1C applies zero volts to the point common to CR1, CR2, and R28. In this condition the voltage at the input to the bipolar ramp generator is dependent on the voltage supplied by the forward voltage source. If both the forward and reverse voltage sources supply zero volt outputs, the input voltage to the bipolar ramp generator will be zero volts and no tape motion will result.

If either the HSREV or REV signal is active (high and low, respectively) or the REV switch is closed, +6.2 volts will be present at the point common to CR1, CR2, and R28. With +6.2 volts present at the junction of CR1, CR2, and R28, a positive voltage is supplied to the bipolar ramp generator input. This results in reverse tape motion at synchronous speed. Variable resistor R28 is used to adjust reverse synchronous tape speed by adjusting the input voltage to the bipolar ramp generator.

When the HSFWD signal is inactive (high) and the +160 switch is in the open position, the output of U1B is zero volts, Q8 is on, C25 has little or no charge, and Q9 is off, supplying zero volts output to the summing junction through R52 and R53. When the HSFWD signal becomes active (low) or the +160 switch is closed, Q8 is cut off and C25 starts to charge toward a voltage somewhere near +3 volts (depending on the setting of variable resistor R53). This draws current through the base-emitter diode of Q9. This current increases as the charge on C25 increases, supplying a positive-going ramp voltage to the summing junction. At the same time, the bipolar ramp generator is supplying a second positive-going ramp voltage to the summing junction because the forward voltage source is activated whenever the high-speed forward ramp circuit is activated. Currents from these two ramp voltages are summed at the summing junction to produce a forward tape speed of greater magnitude than the synchronous speed. The high-speed forward tape speed is adjusted to 160 inches per second by adjusting R53.

Operation of the high speed reverse ramp circuit is similar to that of the high speed forward ramp circuit except that the active level of the HSREV signal is the high level and the ramp voltages supplied to the summing junction by the high speed reverse ramp circuit and the bipolar ramp generator are negative-going ramps.

When the Load Point Search signal is inactive (high), Q12 is on and zero volts is applied to the summing junction. When the Load Point Search signal is active (low), Q12 is off and a positive voltage, sufficient to produce a forward tape speed of

approximately 20 inches per second, is applied to the summing junction through R61 and R63.

A notch filter in the velocity feedback circuit from the tachometer is selected to attenuate the mechanical response of the motor-tachometer combination. A compensating network in the current feedback circuit is also selected, depending upon synchronous speed of the tape unit. When power is removed or tape tension is lost, the return from the capstan motor to the current sense resistor is opened by a relay located on the reel servo printed-circuit assembly.

Dual speed capstan servo amplifier. The primary functional differences between the previously described single-speed capstan servo PCA and the dual-speed capstan servo PCA are as follows: A half speed ramp adjustment variable resistor (R106) is added, in the bipolar ramp generator, between the synchronous-speed ramp adjustment variable resistor and integrating amplifier U3; a second variable resistor (R107) is added between the output of integrating amplifier U3 and the summing junction to enable tape speed adjustment for half-speed operation; and a switching circuit (U1D, U5E, Q14, Q12, and Q13) is added to short out both added variable resistors (R106 and R107) when either high speed forward, high speed reverse, or any density other than 1600 has been selected. The tape will move either forward or reverse (as selected by the FWD and REV signals) at half-speed when neither the HSFWD nor the HSREV signals are active and the D16 signal is active (low). The tape will not run at half-speed when either high speed forward, high speed reverse, or any density other than 1600 has been selected.

4-15. Reel Servo Circuits. The reel servo circuits consist of a tension circuit, a voltage switching circuit, a delay circuit, gain change feedback switches tension arm photosense circuits, preamplifiers, motor power amplifiers, and reel motors. Figure 4-7 is a block diagram of the reel servo circuit.

At initial power-on, the tension circuits disabled. The normally closed contacts of the LOAD pushbutton switch prevent Q13 of the tension circuit from conducting. Pressing the LOAD control allows Q13 to conduct, energizing relay K1. With K1 energized, the capstan and reel servo motor circuits are completed. As tape is tensioned and the tension arms swing away from the limit switches, power through the limit switches maintain a forward bias on Q13 through CR11. When power is removed, or tape tension is lost, the relay is deenergized and is N.C. contacts short across the reel motor windings to provide dynamic braking.

The voltage switching circuit is located on the power regulator printed-circuit assembly. During a high-speed operation forward or reverse, power to the motor power amplifiers is switched from 22.5 volts to 57.5 volts (nominal).

During a high-speed reverse operation (rewind), the HSREV signal from the control and status circuits is gated with the Tension signal. When either tension arm deflects enough both reel motors approach full RPM. On the power regulator P.C.A. the motor voltage exceeds the break-down voltage (10V) of CR4, (power regulator PCA) the condition established by the gating of the HSREV and Tension signals allows current through CR4 to forward bias Q5 voltage switch Q6/Q7 conducts, placing +57.5 volts on the +20/40 line. This applies +40V to the servo amplifier drivers and allows for more power.

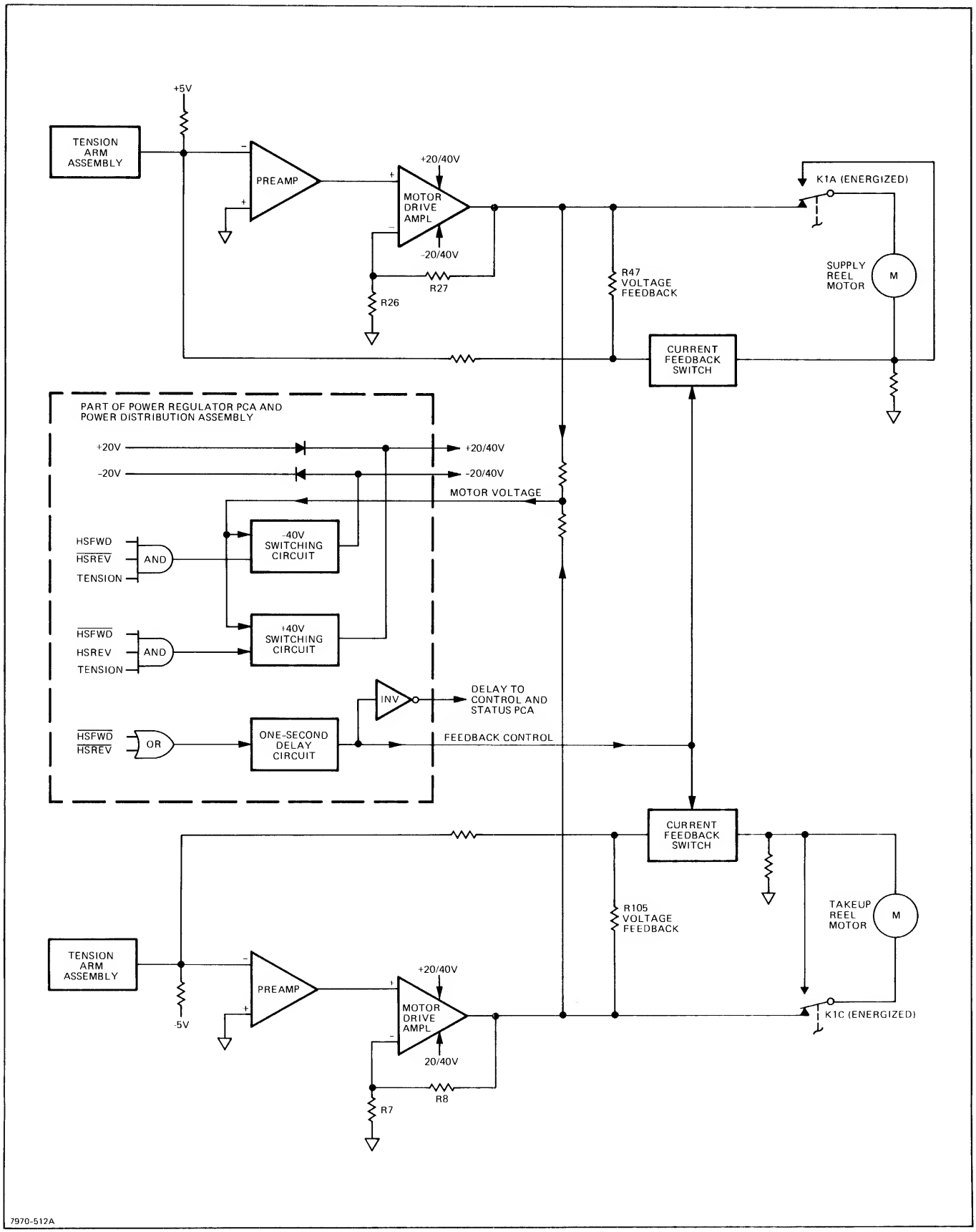


Figure 4-7. Reel Servo Loop, Block Diagram

During a high-speed forward operation, the voltage switching circuits (power regulator PCA) function the same as in the fast reverse operation except that CR6 is used instead of CR4. The HSFWD signal is gated with the Tension signal to allow motor voltage to switch the -40 volt switch (Q12/Q13).

The delay circuit is located on the power regulator printed-circuit assembly. The delay circuit provides an additional one-second delay following the end of a high-speed command. The one-second delay prevents further high-speed commands from the interface from being processed during the one-second period. The one-second delay is also used to switch the reel servo operating mode from high gain back to normal. The switching takes place after reels are slowed.

During normal operation, U5A-3 and U5B-4 (on power regulator PCA) rest at 0 volts. A HSFWD or HSREV signal from the control and status circuits will cut off U5A or U5B and base current for Q15 is supplied through R28 or R29. When Q15 conducts, capacitor C8 immediately discharges through Q15 causing Q16 and Q18 to be cut off. Feedback control to the reel servo changes from approximately +8 volts to approximately -8 volts. The negative potential also reverse biases Q17 and the delay output line switches to +5 volts.

When the high-speed command (HSFWD or HSREV signal) is removed and Q15 loses base current, capacitor C8 is then charged through R33 (one-second time constant). When C8 is charged to +5V, Q16 and Q18 conduct the feedback control changes from -8V to +8 V. The delay output switches to 0 volts.

The reel servo tension arm assemblies contain dual element photo-conductors that are illuminated by a lamp shining through a slotted disc. The slot is in the form of a spiral attached to the tension arm. As the arm moves, the slot exposes different areas of the photo-conductor. As a result, the output of the photo-conductor is proportional to the position of the tension arm.

The reel servo preamplifer is an integrated operational amplifier that amplifies the position error of the tension arm. The tension arm photo-conductor output is single-ended, therefore, an off-set is provided by R39 or R41. The preamplifier drives a class B motor drive amplifier. The motor power amplifier has a gain of 10.

When operating in a normal mode (synchronous or load speed), the servo operates with voltage feedback. The +8 volts from the feedback switching network (feedback control) back-biases the feedback FET switch (Q14 and Q15). Feedback is then provided through R47 and R105. During a high-speed operation, the feedback control changes to -8 volts. The feedback FET switch is forward biased and the feedback voltage path is through the FET switch. On series 1305 and up Q17 thru Q20 makeup a switching network that grounds the output of the preamps when no tape tension exists.

4-16. Control and Status Circuits (Load Function).

The control and status circuits process commands from the front panel controls and interface, and generates controlling signals for the tape transport and data circuits. The control and status circuits also generate status signals for the inter-

face and front panel indicators. The following sequence is the load function. Since it uses the control and status P.C.A. almost completely the discussion will introduce the reader to the sequence of events as well as the control and status PCA.

After power is applied, the tape is not tensioned, limit switch W2S1 is open and the capstan and reel servo circuits are disabled (figure 4-8).

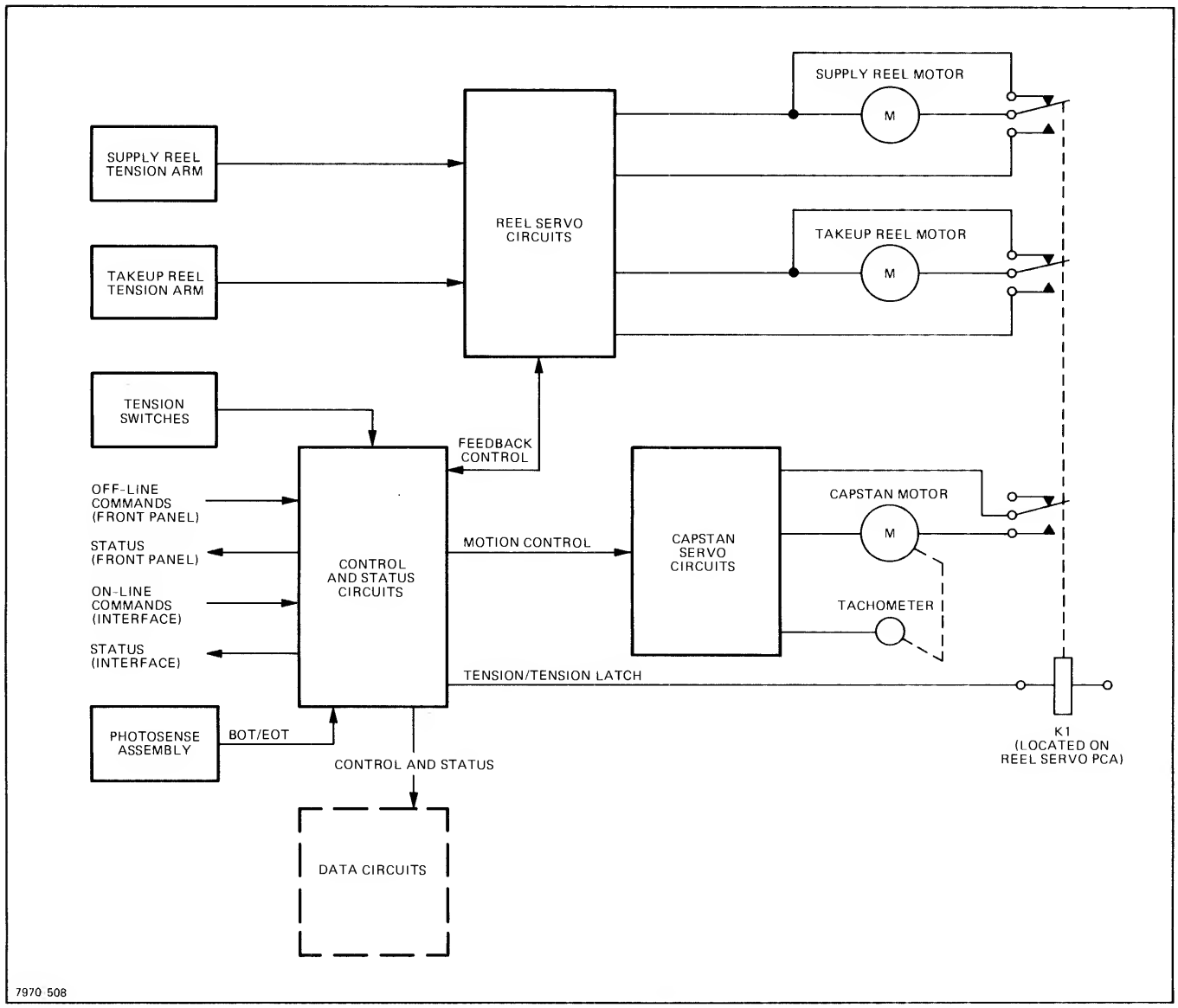


Figure 4-8. Tape Transport Functional Block Diagram

The capstan and reel servo circuits are disabled because relay K1 is deenergized and because ground voltage is supplied to the Tape Tension signal line through the B contacts of deenergized relay K1. Ground voltage supplied to Q4, on the control and status PCA, results in an inactive output from the LDFD FF to the capstan servo circuit. Also, ground voltage supplied to Q22 on the capstan servo PCA (series 1410 and up) holds switch Q20 on the capstan servo PCA closed, grounding the input to motor drive amplifiers Q2, Q4, and Q6. Ground voltage applied to Q19 on the reel servo amplifier PCA, by the Tape Tension signal and through the normally closed contacts of the LOAD switch, cause it to close switches Q16, Q17, and Q20 on the reel servo amplifier PCA. With the inputs to the reel servo amplifiers grounded, the reel motors are disabled. Relay K1 is also kept deenergized through the normally closed contacts of the LOAD switch and Q13 on the reel servo amplifier PCA. When the LOAD switch is pressed, +5 volts is supplied as the Tension signal to Q13 and Q19 on the reel servo amplifier PCA. The high input to Q13 energizes relay K. (Once energized, K1 remains energized, through R109, CR11, and Q13, until tension is lost). Nand gate Q19 holds Q16, Q17, and Q20 open if either of its inputs are high. With K1 energized, both inputs to Q19 are high causing switches Q16, Q17, and Q20 on the reel servo amplifier PCA to open. Thus, both requirements for enabling the reel servos (K1 energized and switches Q16 and Q17 open) are met and the reel servos tension the tape. Thus, with K1 energized and Q20 on the reel servo amplifier PCA open, Q22 on the capstan servo PCA (through Q21) opens Q20 on the capstan servo PCA and enables the amplifier. With tape tension established, tension arm switch W2S1 closes, supplying a high input to terminal D of the Load Forward FF and to Q19 on the reel servo amplifier PCA.

When the LOAD switch is released, the load point search sequence is initiated. Load Latch (U1A and U2A of control and status) is set. The output of the load latch is gated with REW (false) to clock the Load Forward Flip-flop U12A). The LFWD signal is gated with DELAY to provide the capstan servo with the load point search command.

The DELAY signal is generated by a delay circuit located on the power regulator printed-circuit assembly. The delay circuit provides a one-second delay when changing from a high speed operation to a synchronous or load point search mode.

When the load point tab is detected (BOT), the Load Forward flip-flop is cleared by LP through U16D and U13B. Pressing RESET will also clear the Load Forward flip-flop. When Load Forward is cleared, tape load point search motion will stop. The edge transition of LDFD clocks Load Complete flip-flop U12B. Except for a rewind condition, Load Complete remains set during normal operation of the tape transport.

Rewind flip-flop U6B is cleared by pressing the REWIND switch when the unit is off-line, or by interface command REW when the unit is on-line. When the Rewind flip-flop is cleared, the Rewind Status flip-flop (U4B and U3A) is set. This provides rewind status SRW to the interface and rewind status to the control switch assembly to illuminate the REWIND indicator.

When the trailing edge of the load point tab is detected during rewind the Load Point flip-flop is set and the Rewind flip-flop (U6B) is set through te rewind clock input (U6B-11). Load point also gates U3B to prevent rewind commands from clearing the Rewind flip-flop. With the Rewind flip-flop set, the Load Forward flip-flop is set through gate U13A. This starts the load point search mode.

The control and status printed-circuit assembly contains a unit select network that allows up to four units to be controlled by one interface. The network consists of a jumper (W1) and 5 connecting pins (OFF, 0, 1, 2, 3). The position of the jumper determines the unit selected by the interface. If the units connected to the interface are equipped with the unit select switch option, the jumper must be in the OFF position. With the jumper in the OFF position the select match circuitry of the control and status printed-circuit assembly is disabled. If the tape units are not equipped with the unit select switch option, the jumper must be connected to position 0 through 3 depending upon unit designation.

The unit select command from the interface (CS0, CS1, CS2, or CS3) is gated with ON-LINE to generate SOLA and SOLB (U11A and D selected and on-line). The SOLA condition allows status signals to be supplied to the interface. The SOLB condition is gated with COMP (load sequence completed) to generate EXT (external control). The EXT condition allows interface commands to be processed. The OFF-LINE command from the interface does not require the EXT condition. The OFF-LINE command is gated at (U4A) with the unit select command to clear the On-Line latch (UD and U2B).

The Rewind command (REW) from the interface is gated with EXT to clear (assert) the Rewind flip-flop (U6B), provided that tape is not at load point. The forward, reverse, and high-speed (FWD, REV and HIGH SPEED) are gated to provide motion commands to the tape transport servos and data circuits.

All status signals to the interface are gated with SOLA. The load point status (SLP) indicates that the tape unit is at load point (load point tab under photosense head). The end-of-tape status (SET) indicates that the tape is at or beyond the end-of-tape tab. The rewind status (SRW) indicates that the tape is rewinding or in an automatic load point search operation. The ready status (SR) indicates that the tape unit is selected, on-line, and that the load sequence is complete (not rewinding and not in a load point search mode). The on-line status (SL) and file protect status (SFP) indicate that the unit is on-line, and that the tape reel installed on the supply reel hub is not equipped with a write enable ring.

4-17. NRZI Read Circuits Discussion.

The following discussion is referenced to the enclosed block diagrams, the parts and diagrams manual, and to specific paragraphs (as called out) elsewhere in this manual. The discussion of the Read circuitry is in a functional block diagram. Since the NRZI Read format is almost identical in a 7970B and a 7970E, the discussion is based on the B format and any deviations in the E are noted as such. The Reader is left with correlating the functional blocks with the detail at schematic level. Examples are given at various points in the discussion to ensure the reader gets the feel of the transition from block diagram to schematic diagram.

The read modules consist of the read magnetic head assembly, a read preamplifier printed-circuit assembly, a read assembly and a density select assembly. The magnetic head assembly is a seven and or nine track read, NRZI or PE head. Channel scrambling is accomplished in the head assembly wiring. From the reference edge of the tape (edge facing the operator) the nine-track channel designations are 5, 7, 3, P, 2, 1, 0, 6, and 4. The seven-track channel designations are 7, 6, 5, 4, 3, 2, and P.

The NRZI read circuits are illustrated in block diagram, figure 4-9.

The read assembly consists of a card cage assembly (motherboard) that contains a read/read control printed-circuit assembly, a single-channel read data printed-circuit assembly and three dual-channel read data printed-circuit assemblies.

The density select switch assembly allows the operator to select read densities of 200, 556, or 800 cpi. The assembly consists of a three-button, interlocked switch assembly with indicators and a printed-circuit assembly that contains line-drivers. A separate switch and indicator on the assembly allows selection of seven- or nine-track operation.

4-18. Functional Description.

Information to be read from the magnetic tape has been recorded in NRZI (non-return-to-zero-ones inverted) form, in seven or nine tracks. A "one" bit is represented by a flux reversal and a "zero" bit is represented by the absence of a flux reversal. The character bytes are recorded at a density of 200, 556, or 800 character bytes per inch (cpi).

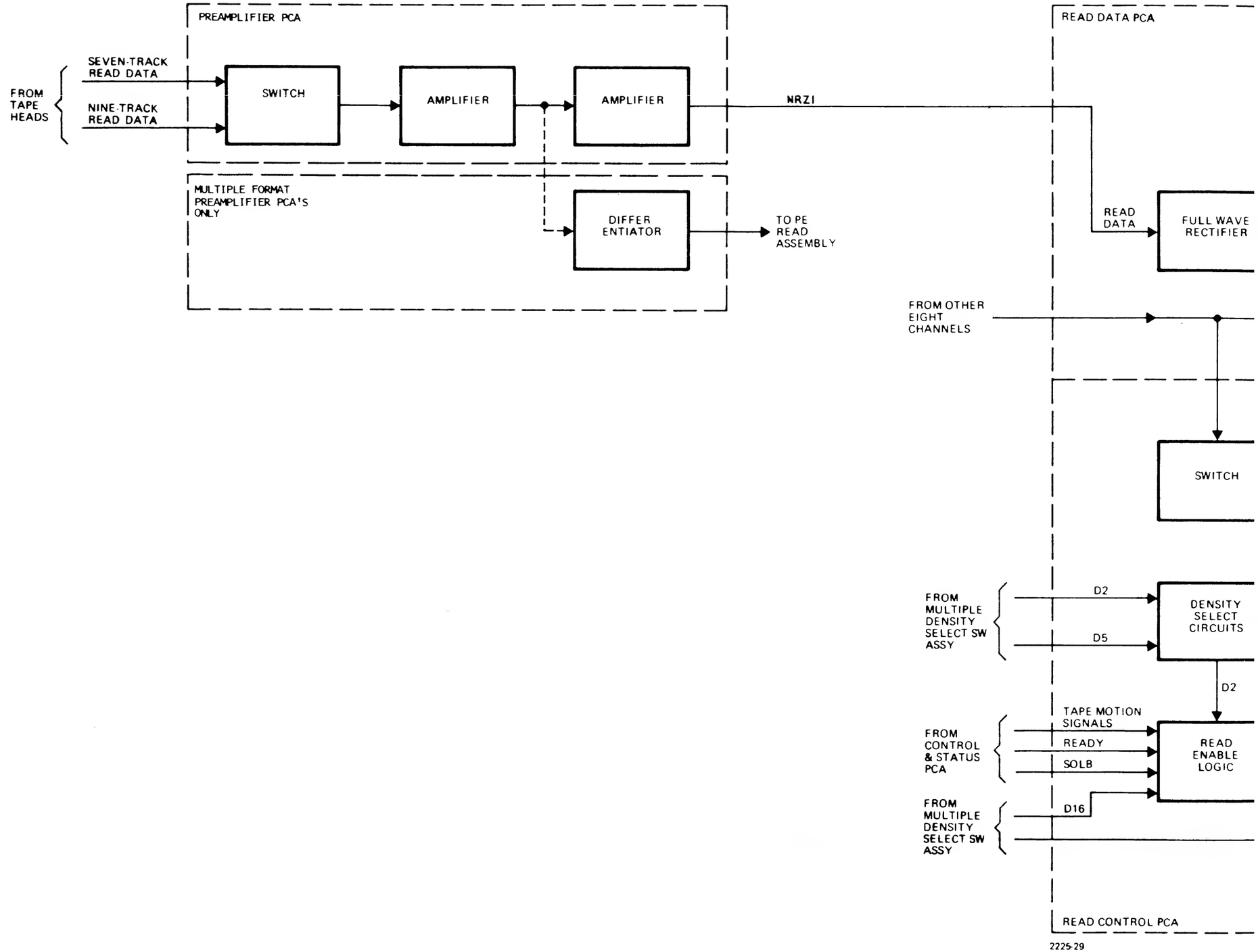
See paragraph 4-2 for more detail on NRZI format.

The preamplifier PCA (7970E may have a multiple format preamplifier PCA) receives the input read data from the tape heads. A switch circuit selects either seven-track or nine-track data as the source data, depending on whether the S7T signal is active or inactive. The preamplifier amplifies both NRZI and/or PE data. When the NRZI circuits are selected for operation, the PE read circuits will not be active on multi/format. In the preamplifier the NRZI data is amplified only. Differentiation of the NRZI data is accomplished on the NRZI read PCA's. (The PE read data is both amplified and differentiated on the PE preamplifier.)

The input read data from the preamplifier to the read data PCA is in the form of positive and negative peaks, each of which represents a "1" (see figure 4-6). The "1's" are converted to positive peaks by a fullwave rectifier located on the read data PCA. A threshold voltage, generated by circuits on the read control PCA, is supplied to the read data PCA. This guards succeeding circuits against noise triggering (false logic 1's). The positive peaks of the input data, which represent the time of occurrence of "1's", are converted to zero crossings (crossings of the zero volts line) by a peak detector circuit. A high-gain amplifier converts the resulting waveform into a digital waveform with positive excursions occurring in place of the zero crossings. This digital waveform is supplied to skew-delay RC circuit. See figure 4-10.

In 7970B (NRZI) the skew-delay RC circuit receives reference power from the read control PCA. (Read FWD or Read REV).

In 7970E multiformat the skew-delay RC circuit receives reference power from the 7TR/9TR switch through either the 7-track or 9-track signal on the NRZI read control PCA. This signal is used to generate a ramp waveform, beginning when the zero crossing (logic 1) occurs. The ramp voltage is sensed by a threshold switch which shorts the ramp voltage to approximately ground voltage when a threshold voltage is reached. The time between the beginning and end of the ramp voltage can be


PREAMPLIFIER PCA
SEVEN-TRACK READ DATA
NINE-TRACK READ DATA
FROM TAPE HEADS
SWITCH
AMPLIFIER
AMPLIFIER
NRZI
MULTIPLE FORMAT PREAMPLIFIER PCA'S ONLY
DIFFER ENTIATOR
TO PE READ ASSEMBLY
READ DATA PCA
READ DATA
FULL WAVE RECTIFIER
FROM OTHER EIGHT CHANNELS
SWITCH
FROM MULTIPLE DENSITY SELECT SW ASSY
D2
D5
DENSITY SELECT CIRCUITS
D2
TAPE MOTION SIGNALS
READY
SOLB
FROM CONTROL & STATUS PCA
D16
FROM MULTIPLE DENSITY SELECT SW ASSY
READ ENABLE LOGIC
READ CONTROL PCA

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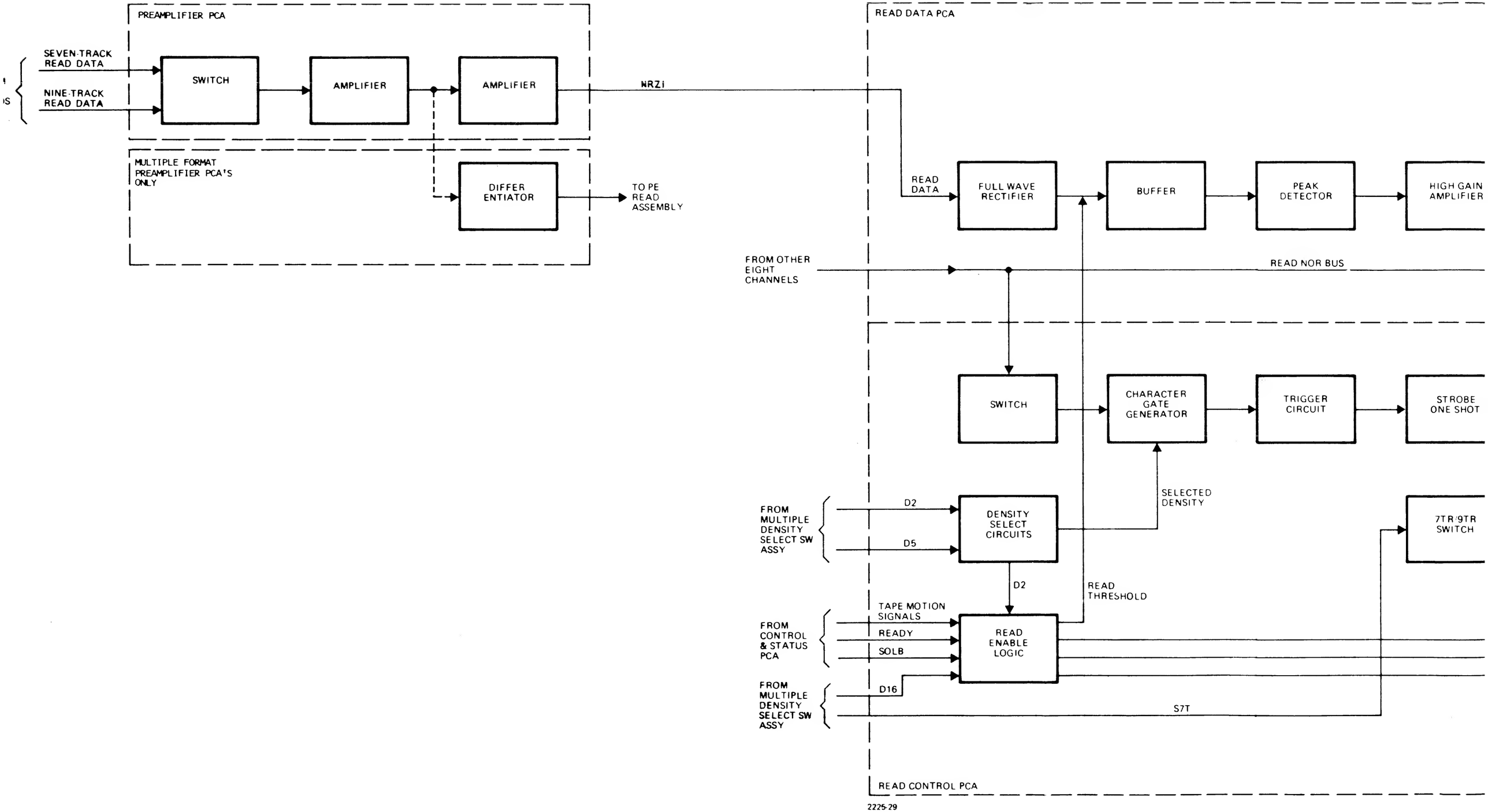
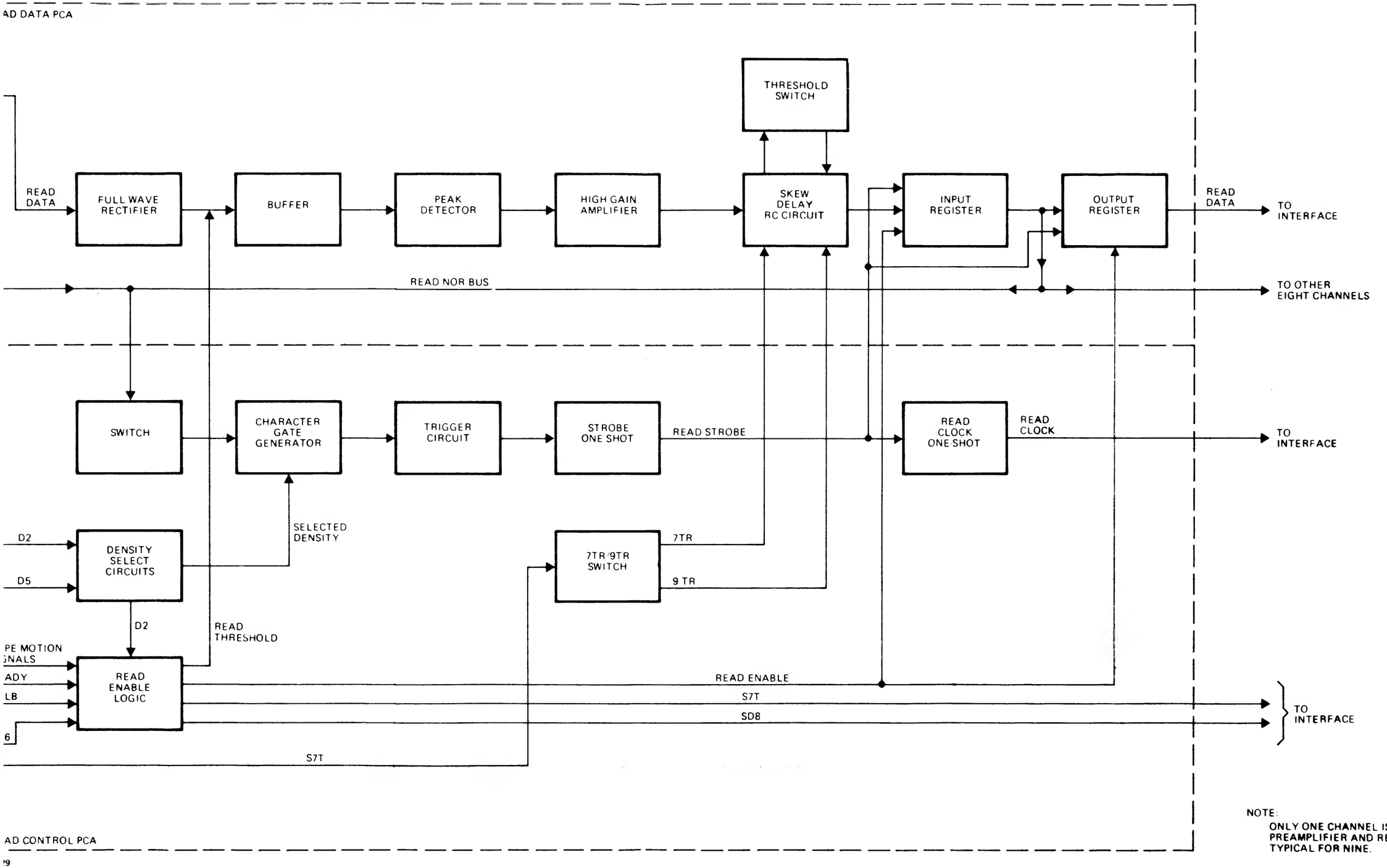

PREAMPLIFIER PCA
SEVEN-TRACK READ DATA
NINE-TRACK READ DATA
SWITCH
AMPLIFIER
AMPLIFIER
NRZI
MULTIPLE FORMAT PREAMPLIFIER PCA'S ONLY
DIFFER ENTIATOR
TO PE READ ASSEMBLY
READ DATA PCA
READ DATA
FULL WAVE RECTIFIER
BUFFER
PEAK DETECTOR
HIGH GAIN AMPLIFIER
FROM OTHER EIGHT CHANNELS
READ NOR BUS
SWITCH
CHARACTER GATE GENERATOR
TRIGGER CIRCUIT
STROBE ONE SHOT
SELECTED DENSITY
FROM MULTIPLE DENSITY SELECT SW ASSY
D2
D5
DENSITY SELECT CIRCUITS
7TR/9TR SWITCH
D2
READ THRESHOLD
FROM CONTROL & STATUS PCA
TAPE MOTION SIGNALS
READY
SOLB
READ ENABLE LOGIC
FROM MULTIPLE DENSITY SELECT SW ASSY
D16
S7T
READ CONTROL PCA
2225-29



NOTE:
ONLY ONE CHANNEL IS SHOWN THROUGH THE PREAMPLIFIER AND READ DATA PCA AS TYPICAL FOR NINE.

Figure 4-9. NRZI Read Circuits Block Diagram

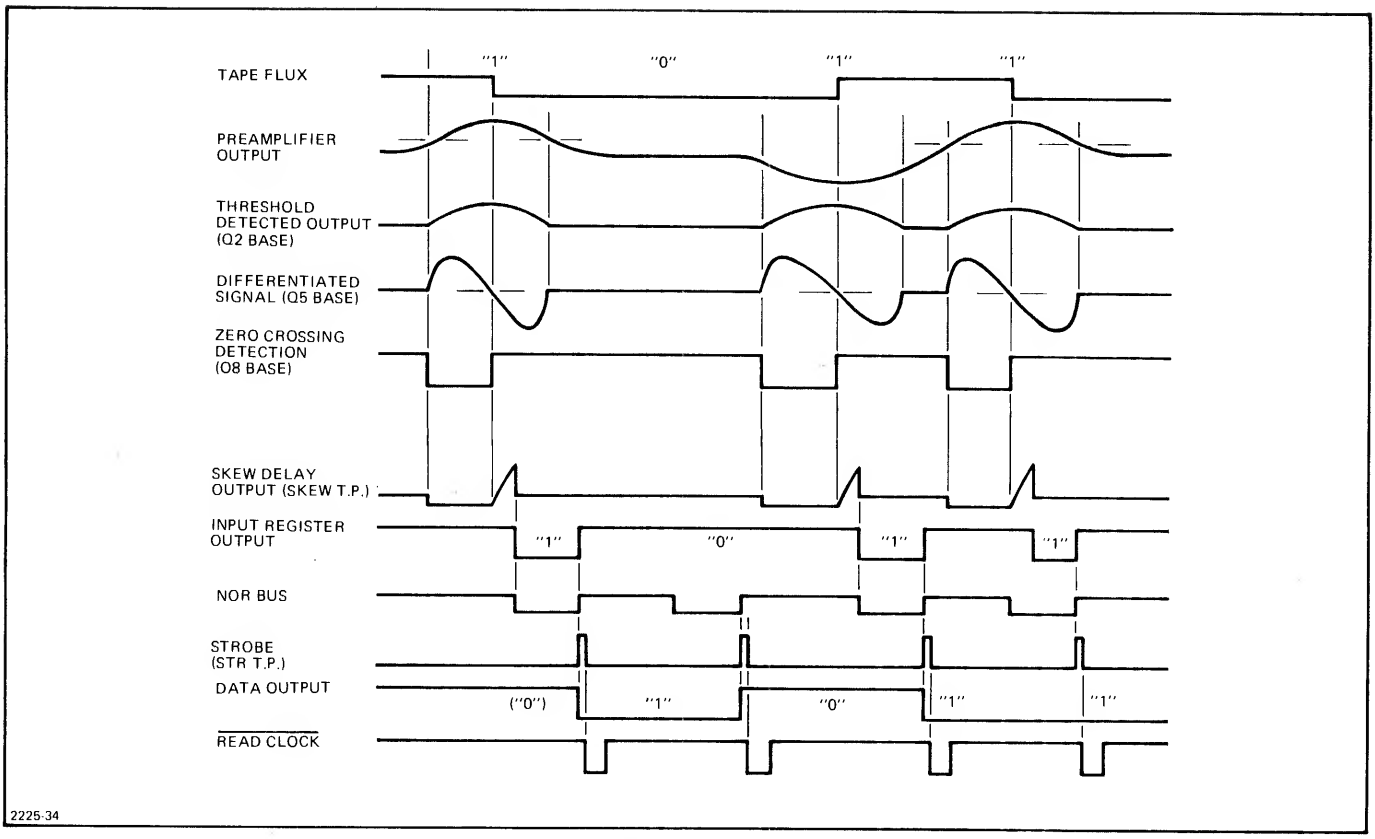


Figure 4-10. NRZI Circuits Waveforms

varied by adjusting the slope of the ramp. Skew adjustment is made by adjusting the ramp for each channel so that all ramp voltages terminate at the same time.

When a data "1" bit is processed through the input and delay circuits, the input register stores a "1" and activates the read "nor" bus. The "nor" bus receives signals form the input register of all nine channels. Therefore, it will be activated by the first channel which receives a "1". When the read "nor" bus is activated, the character gate generator on the read control PCA begins a voltage ramp which determines the length of the character gate. When the ramp reaches a threshold, the trigger circuit activates the Strobe one-shot multivibrator to generate the Read Strobe signal. The character gate begins when the read "nor" bus becomes active and ends when the Read Strobe signal becomes active. It is adjustable and is normally adjusted to be 45 percent of the nominal byte time. However, the byte time is different for different densities and tape speeds. Therefore, the character gate must be adjusted according to the tape speed and density of the tape data. The density select circuits indicate to the character gate generator the density selected on the multiple density select switch assembly. The character gate determines the length of time the "nor" bus is active.

When the Read Strobe signal is generated, a "1" or "0" is stored in the output register depending on whether or not a "1" is stored in the input register. Also, the input register is cleared at the same time. When the short duration Read Strobe signal ends, the Read Clock one-shot multivibrator generates the Read Clock signal which clocks the data bit present in the output register into the interface.

If a "0" occurs at the input of the read data PCA, the full wave rectifier, buffer, peak detector, high-gain amplifier, skew delay RC circuit, threshold generator, and input register will remain inactive. Since the input register has not stored a "1", when the Read Strobe occurs, a "0" will be stored in the output register and clocked out to the interface. The read control circuits operate as previously described to produce the Read Strobe because a "1" must occur on at least one of the nine channels for every byte.

4-19. PE Read Circuits Overall Functional Sequence Explanation.

The PE read circuits are state controlled. When the machine is in any given state it is given certain directions and makes certain decisions. The results of the decisions advances the machine to another operation or another state. State control logic sequences the activities of the data path circits during any PE Read operation. This data path consists of the Decoder, Data and Status, and the Read Control PCA's. The final decision is made when the proper conditions exist to generate output signals.

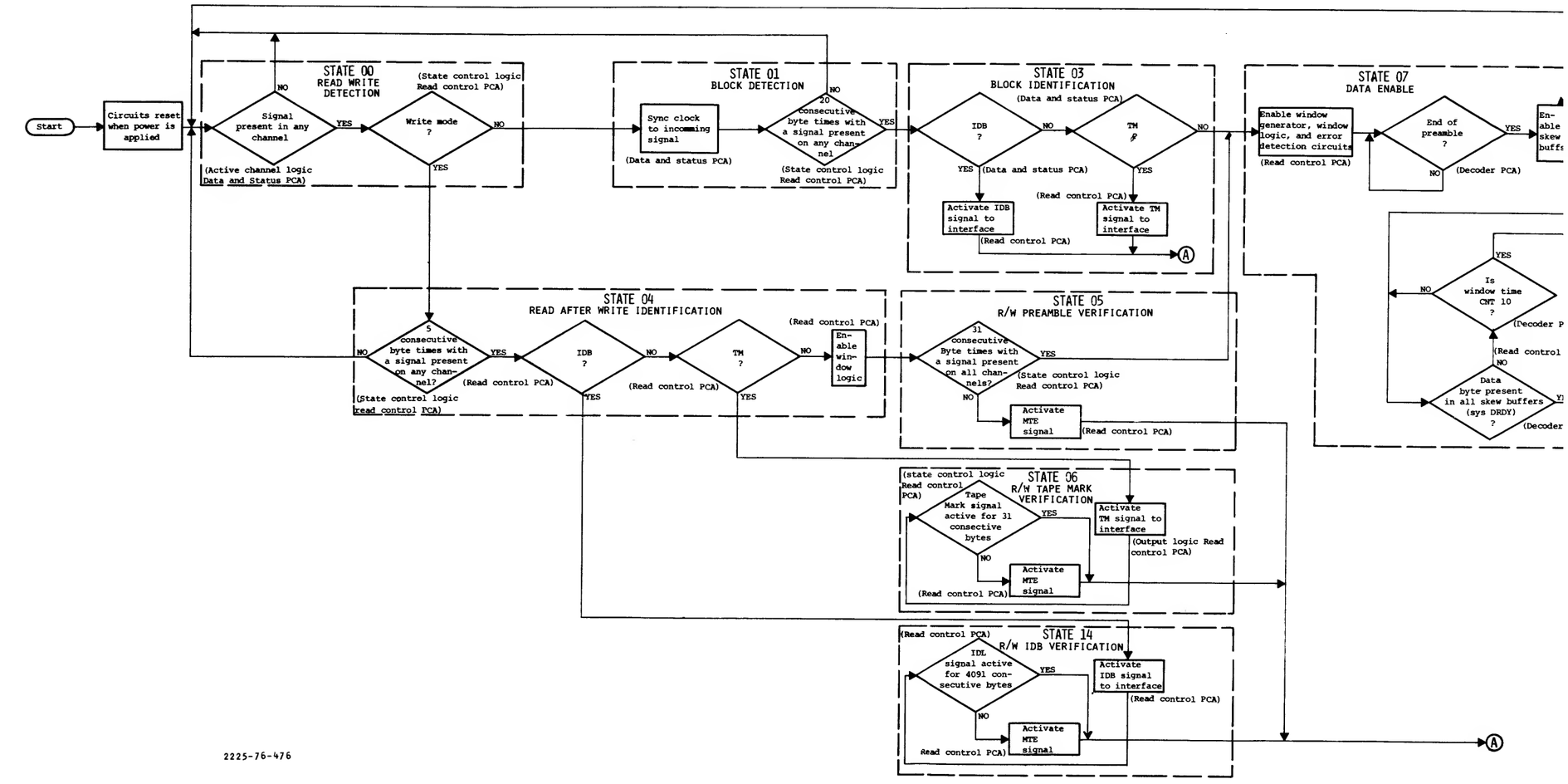
The PE read circuits operate in two modes; read only and read after write. Signals read off tape in read after write mode are required to meet more stringent requirements, before being recognized as valid than read only mode signals. This ensures reliability and compatability to industry standards.

Figure 4-11 is a flow diagram which is laid out and itemized to show the direct correlation of the state decisions to the logic shown on the schematics of the PCA's. (Refer to parts and diagrams manual). Each decision block within each state has a notation showing which PCA makes that decision, often the area on the PCA schematic is included.

4-20. PE Read Circuits State Control Sequence Discussion.

When power is applied to the PE read circuits, most sequencing and output circuits are reset, (State counter is reset at 0000). When a signal is detected in any of the nine channels, a check is made to determine if the PE read circuits are operating in read only or read after write mode. (State 00) refer to figure 4-11.

To show the use of the flow diagram in conjunction with the diagrams manual, let's say in the above decision we are in the Read after Write mode: The state counter advances from 00 to 04. (The state counter is discussed in the following information) once in state 04 (S04) the next decision is; do we have 5 consecutive byte times with a signal present on any channel? As shown on the flow diagram, this decision is made on the Read Control PCA and specifically in the state control logic. If we now refer to the read control PCA shcematic, the output of U27C is S04


Start
Circuits reset when power is applied
STATE 00
READ WRITE DETECTION
Signal present in any channel
NO
YES
Write mode ?
NO
YES
(State control logic Read control PCA)
(Active channel logic Data and Status PCA)
STATE 01
BLOCK DETECTION
Sync clock to incomming signal
(Data and status PCA)
20 consecutive byte times with a signal present on any channel
NO
YES
(State control logic Read control PCA)
STATE 03
BLOCK IDENTIFICATION
(Data and status PCA)
IDB ?
NO
YES
(Data and status PCA)
TM ?
NO
YES
(Read control PCA)
Activate IDB signal to interface
(Read control PCA)
Activate TM signal to interface
A
STATE 07
DATA ENABLE
Enable window generator, window logic, and error detection circuits
(Read control PCA)
End of preamble ?
YES
NO
(Decoder PCA)
En-able skew buffs
STATE 04
READ AFTER WRITE IDENTIFICATION
5 consecutive byte times with a signal present on any channel?
NO
YES
(Read control PCA)
IDB ?
NO
YES
(Read control PCA)
TM ?
NO
YES
(Read control PCA)
En-able win-dow logic
(State control logic read control PCA)
STATE 05
R/W PREAMBLE VERIFICATION
31 consecutive Byte times with a signal present on all channels?
YES
NO
(State control logic Read control PCA)
Activate MTE signal
(Read control PCA)
Is window time CNT 10 ?
YES
NO
(Decoder P
(Read control
Data byte present in all skew buffers (sys DRDY) ?
NO
YES
(Decoder
(state control logic Read control PCA)
STATE 06
R/W TAPE MARK VERIFICATION
Tape Mark signal active for 31 consective bytes
YES
NO
Activate TM signal to interface
(Output logic Read control PCA)
Activate MTE signal
(Read control PCA)
(Read control PCA)
STATE 14
R/W IDB VERIFICATION
IDL signal active for 4091 consecutive bytes
YES
NO
Activate IDB signal to interface
(Read control PCA)
Activate MTE signal
Read control PCA)
A

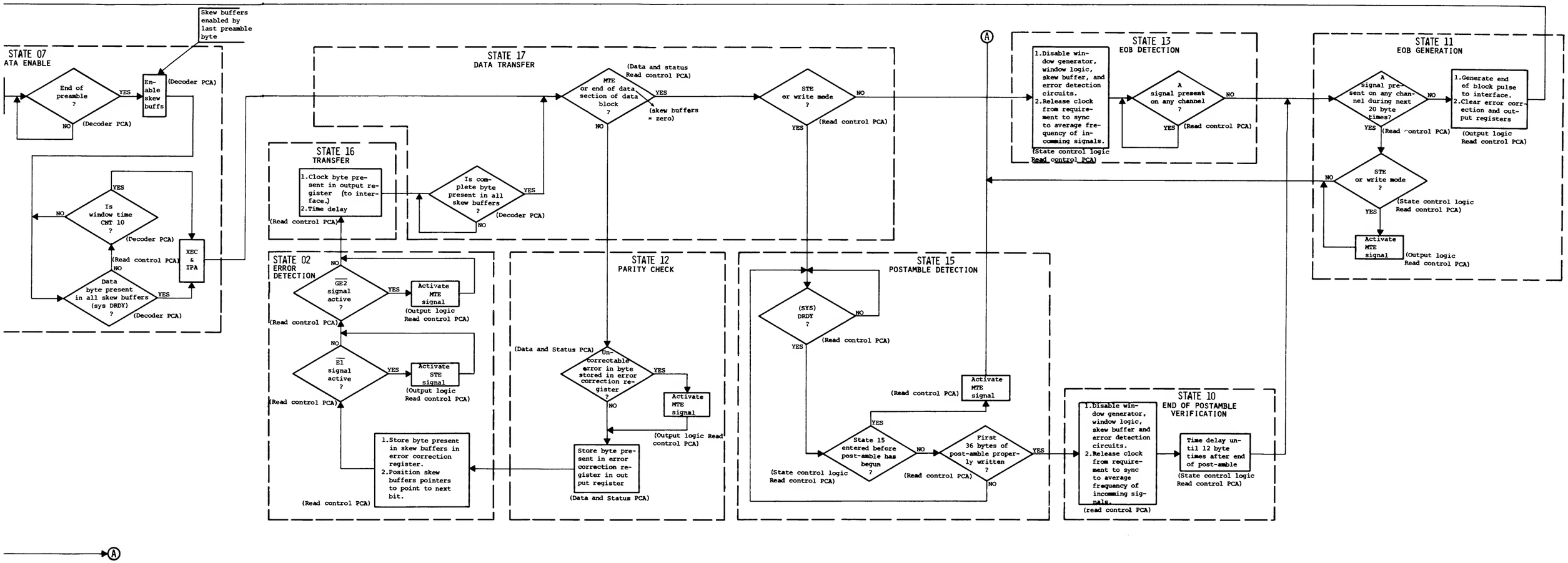


Figure 4-11. PE State Control Flow Diagram

and count 5 (cnt 5) and signal present any channel (ANYL). (S04-CNT5-ANYL). If either CNT 5 or ANYL is a false or low signal, then this would correspond to a "NO" decision on the flow diagram. By NORING this output (false) at U44A with the term CNT36 we have two low signals on the input and a high on the output. The high output resets U111B (22FF) and the state count goes from 4 (0100) to zero (0000).

Now look at U310A of the read control PCA. It's output reads CNT5 and S04. This output goes to NAND GATE U38A and is gated with Identification signal (IDL). If this output is true the U111A (23FF) is set. This is a yes decision for the first two decisions on the flow diagram in state 04. Thus, the true output (U111A) causes the counter to go from S04 (0100) to S14 (1100), as indicated on the flow diagram.

The discussion above relates the method of using the flow diagram and the schematics for detailed circuit troubleshooting.

4-21. PE Read Circuits Overall Functional Discussion.

This discussion will reference to the previous state control logic explanation and the parts and diagrams manual. Also use paragraphs 4-2 and 4-3 as reference for general PE Code and tape information.

The following paragraphs trace signal flow from the tape heads to the interface. The discussion is based on the PE read circuits block diagram (figure 4-12). Paragraph 4-22 describes signal flow from the preamplifier to the level change register. Paragraph 4-23 traces the signal path from the threshold comparator to the amplitude detector, to produce the Level signal (the Level signal is required to enable other circuits), and through the sync generator and clock control circuits to the clock to produce the DF and 40 DF pulse trains. The DF and 40 DF pulse trains synchronize the PE read circuits. Paragraph 4-24 describes both operation of the circuits (amplitude detector, active channel logic, state control logic, and window generator) and the conditions required to activate and unlock the pointer register enable latch and enable the window logic, the pointer register enable latch must be unlocked to enable the skew buffer and the window logic must be enabled to produce the Shift signal which shifts data from the level change register into the skew buffer. Paragraph 4-25 provides a brief explanation of skew buffer operation. Then paragraph 4-26 describes operations of the error-correction register, parity checker, error correction circuits, and output register. Operation of the skew buffer output sensing circuits, end of data logic, state control logic, and output logic (which becomes significant during reading of the postamble) is described in paragraph 4-27. Paragraph 4-28 describes functions of the error detection circuits and the TIE decoder logic.

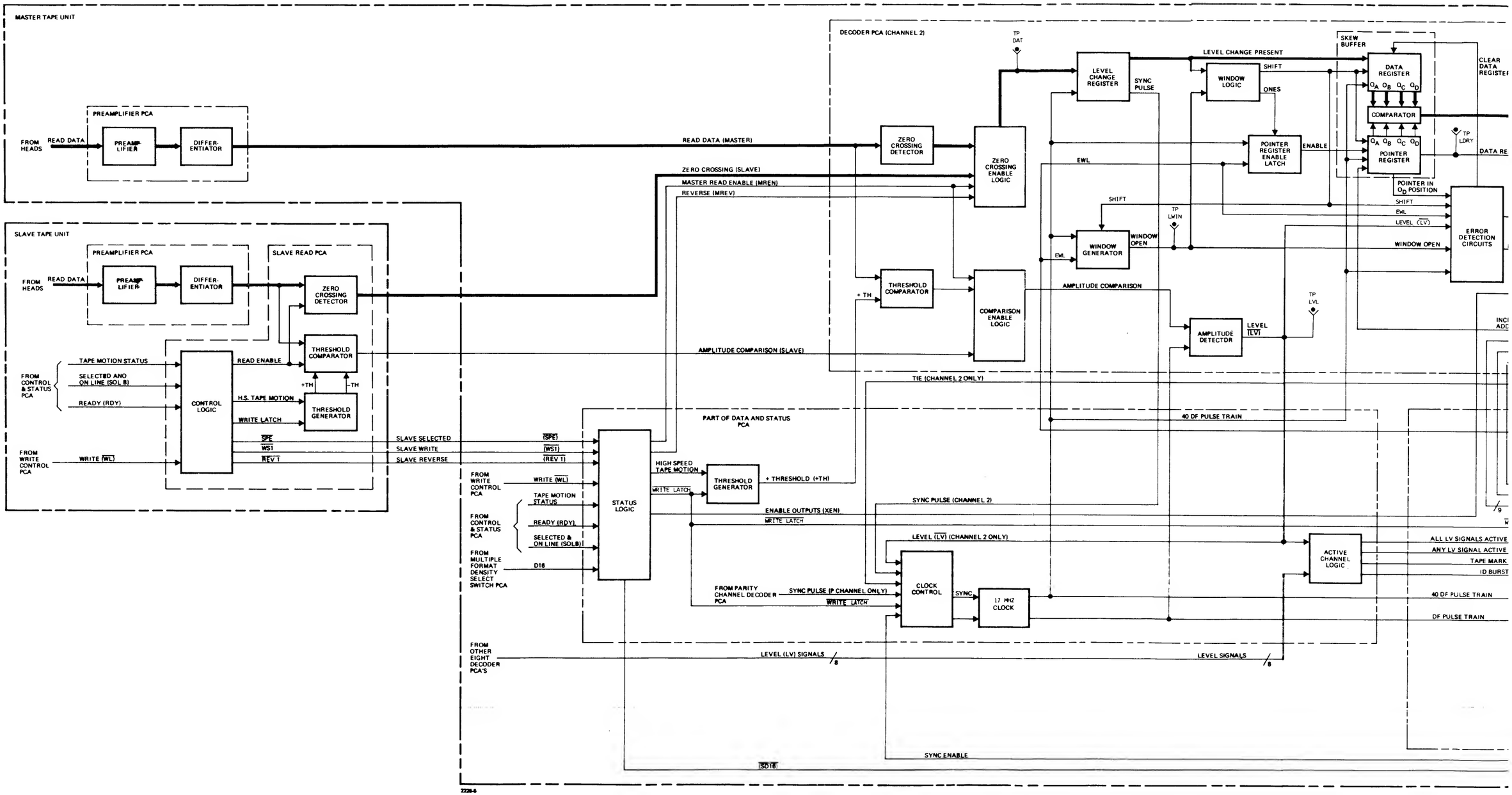
4-22. Signal Flow (Preamplifier to Level Change Register). The flow of signals through the PE read circuits (figure 4-12 and 4-13) is from the tape heads, through the preamplifier, differentiator and zero crossing detector. (These circuits might be located in either the master or slave tape unit, depending on which is supplying the signals. If a slave unit is supplying the signals, the signals enter the master tape unit after being digitized by the zero crossing detector).

The signals are amplified by the preamplifier, the differentiator produces a crossing of the zero volts line for each tape flux reversal (peak), and the zero crossing detector digitizes the amplitude-varying signal from differentiator to produce logic 1's and 0's. If a slave tape unit is supplying the signals, they pass through the zero crossing enable logic to the level change register without restriction. However, if the master unit is providing the signals, the Master Read Enable (MREN) signal must be active to enable passage of the signals through the zero crossing enable logic. The MREN signal, which originates in the status logic on the data and status PCA, is active when the master tape unit is selected and on-line, the tape is moving and is past the beginning of tape (BOT) marker, and density 1600 is selected. The Read Enable signal generated by the control logic in the slave unit performs a function similar to the MREN signal in the master tape unit. The signals from zero crossing enable a logic one to be stored, momentarily, in the level change register as level changes (or level transitions). While in the level change register, the signals are applied, as the Level Transitions signal, to the skew buffer. However, the skew buffer can take no action until the pointer register enable latch and window logic are enabled.

4-23. Signal Flow (Threshold Comparator to Amplitude Detector, Sync Generator, and Clock). The output of the differentiator, in addition to being applied to the zero crossing detector, is also applied to the threshold comparator (in either the master or slave tape unit). The amplitude of the signal is compared, in the threshold comparator, with positive and negative thresholds generated by the threshold generator. (The thresholds are higher, requiring greater signal amplitude, in read-after-write mode). If the signal is of sufficient amplitude, to exceed the threshold, a digitized Amplitude Comparison (AC) signal is supplied by the comparision enable logic to the amplitude detector and sync generator. If the master tape unit is reading the tape, the MREN signal must be active for the comparison enable logic to pass the signal. This is not necessary if a slave unit is reading the tape. However, the same function is performed in the slave PE read circuits.

When the output of the differentiator is of insufficient amplitude to exceed the threshold level for three consecutive DF periods, the amplitude detector inhibits action of the window logic (the window logic must be enabled for data to pass through the decoder PCA) and notifies the error detection circuits in the channel logic, on the data and status PCA, that the channel with which it is associated has no threshold-exceeding input. The amplitude detector (for channel two only) also informs the clock control logic that channel two is receiving no threshold-exceeding input.

The channel two and channel P sync generators supply a Sync Pulse to the clock control circuits, for every level change (level transition) entering the level change register. This includes both transitions representing a logic 1 or logic 0 and phase correction transitions. The clock uses these pulses to determine the average length of time between bytes and adjusts the time of a Data Frequency period to this time. The clock, on the data and status PCA, generates two pulse trains; the data frequency (DF) pulse train and the 40 DF pulse train. Both are used to synchronize operation of the master PE read circuits. The 40 DF pulse train has a frequency 40 times greater than the DF pulse train. Thus, forty 40 DF pulses occur for each DF pulse. (The frequency of the 40 DF pulse train is also adjusted to agree with the average byte time).


MASTER TAPE UNIT
PREAMPLIFIER PCA
FROM HEADS
READ DATA
PREAMP-LIFIER
DIFFER-ENTIATOR
SLAVE TAPE UNIT
PREAMPLIFIER PCA
SLAVE READ PCA
ZERO CROSSING DETECTOR
THRESHOLD COMPARATOR
+TH
-TH
THRESHOLD GENERATOR
FROM CONTROL & STATUS PCA
TAPE MOTION STATUS
SELECTED AND ON LINE (SOL B)
READY (RDY)
CONTROL LOGIC
READ ENABLE
H.S. TAPE MOTION
WRITE LATCH
FROM WRITE CONTROL PCA
WRITE (WL)
SPE
WS1
REV 1
SLAVE SELECTED
SLAVE WRITE
SLAVE REVERSE
READ DATA (MASTER)
ZERO CROSSING (SLAVE)
MASTER READ ENABLE (MREN)
REVERSE (MREV)
AMPLITUDE COMPARISON (SLAVE)
DECODER PCA (CHANNEL 2)
TP DAT
ZERO CROSSING DETECTOR
ZERO CROSSING ENABLE LOGIC
THRESHOLD COMPARATOR
+ TH
COMPARISON ENABLE LOGIC
LEVEL CHANGE REGISTER
SYNC PULSE
LEVEL CHANGE PRESENT
WINDOW LOGIC
SHIFT
ONES
SKEW BUFFER
DATA REGISTER
O_A O_B O_C O_D
COMPARATOR
POINTER REGISTER ENABLE LATCH
ENABLE
POINTER REGISTER
TP LDRY
CLEAR DATA REGISTER
DATA RE
POINTER IN O_D POSITION
SHIFT
EWL
LEVEL (LV)
WINDOW OPEN
ERROR DETECTION CIRCUITS
EWL
WINDOW GENERATOR
WINDOW OPEN
TP LWIN
AMPLITUDE COMPARISON
AMPLITUDE DETECTOR
LEVEL (LV)
TP LVL
TIE (CHANNEL 2 ONLY)
40 DF PULSE TRAIN
PART OF DATA AND STATUS PCA
STATUS LOGIC
FROM WRITE CONTROL PCA
WRITE (WL)
FROM CONTROL & STATUS PCA
TAPE MOTION STATUS
READY (RDY)
SELECTED & ON LINE (SOL B)
FROM MULTIPLE FORMAT DENSITY SELECT SWITCH PCA
D16
HIGH SPEED TAPE MOTION
WRITE LATCH
THRESHOLD GENERATOR
+ THRESHOLD (+TH)
ENABLE OUTPUTS (XEN)
WRITE LATCH
SYNC PULSE (CHANNEL 2)
LEVEL (LV) (CHANNEL 2 ONLY)
FROM PARITY CHANNEL DECODER PCA
SYNC PULSE (P CHANNEL ONLY)
WRITE LATCH
CLOCK CONTROL
SYNC
17 MHZ CLOCK
ACTIVE CHANNEL LOGIC
ALL LV SIGNALS ACTIVE
ANY LV SIGNAL ACTIVE
TAPE MARK
ID BURST
40 DF PULSE TRAIN
DF PULSE TRAIN
FROM OTHER EIGHT DECODER PCA'S
LEVEL (LV) SIGNALS
8
LEVEL SIGNALS
8
SYNC ENABLE
SD16
2228-6

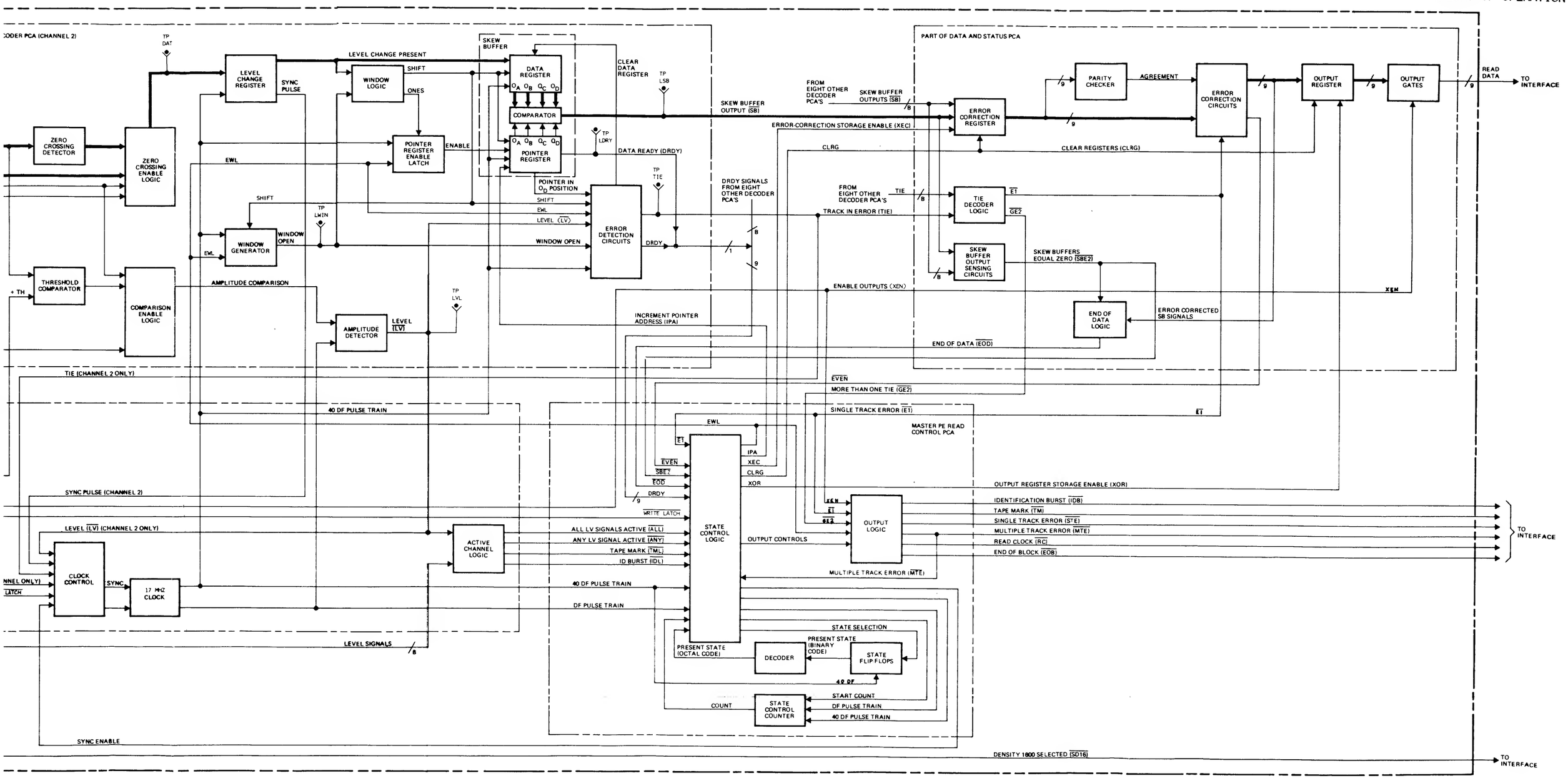


Figure 4-12. PE Read Circuits Block Diagram

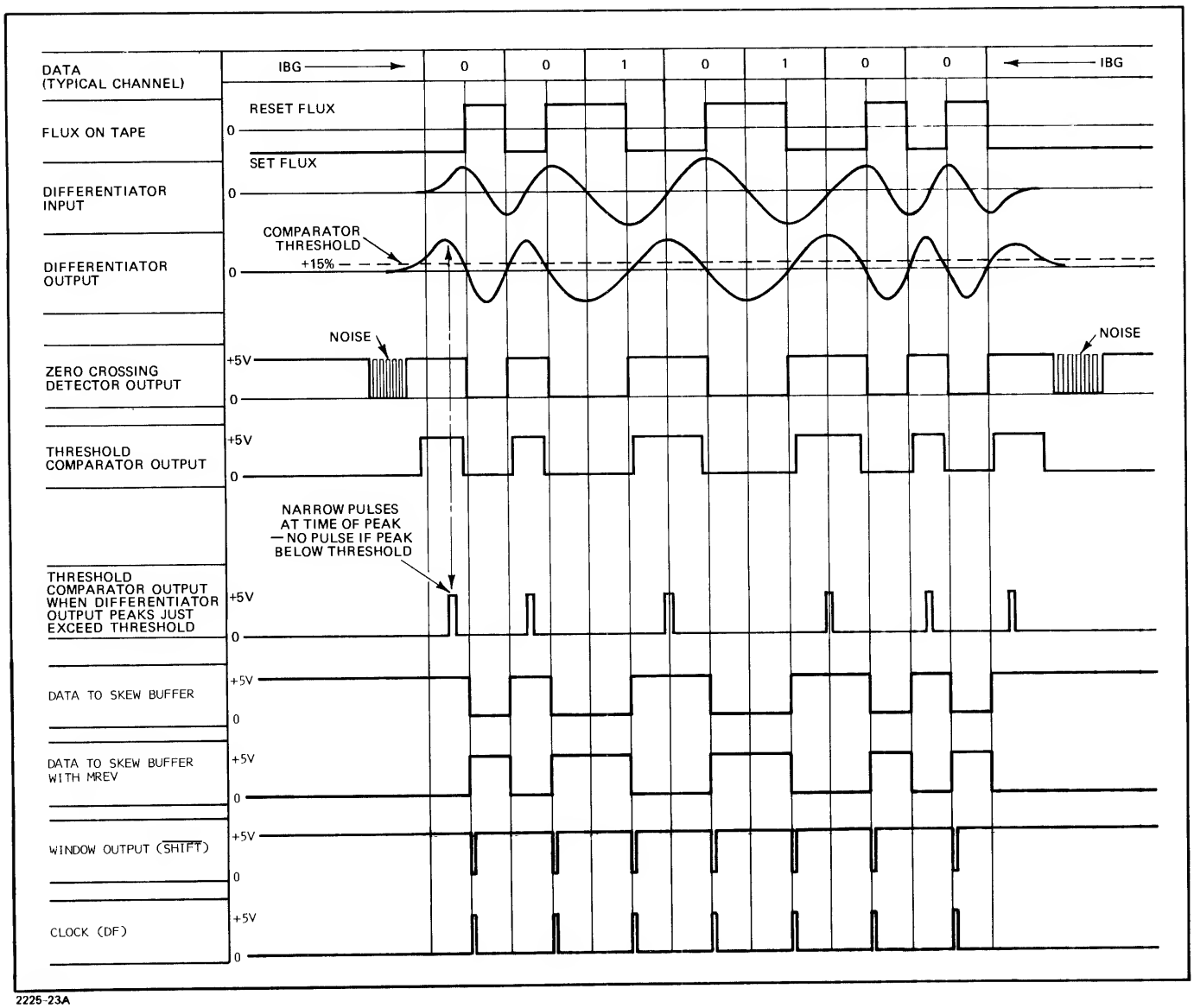


Figure 4-13. PE Circuits Waveforms

The clock control circuits are informed, by the Write signal from the status logic, whether or not the PE read circuits are operating in read-after-write mode. The Sync Enable signal from the state control logic informs them when certain conditions exist in read-only mode. When these conditions exist in read-only mode, the clock control circuits notify the clock and supply it with Sync pulses. When it receives the enabling signal and Sync pulses, the clock synchronizes to the average frequency

of the incoming signal. In read-after-write mode and under certain conditions in read-only mode, the clock operates at a fixed frequency.

In read-only mode (under certain conditions) the clock control circuits supply the Sync Pulses from channel two to the clock, provided they have not received notice from the channel two amplitude detector that channel two is not receiving a signal or from the channel two error detection circuits that channel two is in error. The clock uses these Sync Pulses to determine the average byte time of the incoming Read signals and adjusts the DF and 40 DF pulse trains accordingly. However, if channel two is receiving no threshold-exceeding signal or is in error, the clock control circuits will supply the Sync Pulses from channel P to the clock instead of the channel two pulses.

In read-after-write mode, if no input is received from the tape, and under certain conditions in read-only mode, the clock operates at a fixed frequency. In read-only mode, the clock averages the frequency of the incoming signal on either channel two or channel P (parity channel) and operates at the average frequency. The selection of either channel two or channel P as the reference channel is made by the clock control circuits.

4-24. Enabling the Window Logic and Skew Buffer. The signals from the zero crossing enable logic, in the form of level changes (or transitions), are stored, momemtarily (for one 40 DF period), in the level change register. While in the level change register, they are applied to the sync generator, error detection circuits, skew buffer, and window logic. However, before the level transitions can be acted upon by the skew buffer, the skew buffer must be enabled by the Enable signal from the pointer register enable latch. Also, once enabled, the skew buffer requires an active Shift pulse from the window logic to store new data bits (and shift data bits from previous bytes, when any are present in the skew buffer). Thus, the window logic must also be enabled.

A number of conditions must be met to enable the window logic, activate the Enable signal from the pointer register enable latch, and thus enable operation of the skew buffer. These conditions are detailed in the following paragraphs.

Both the Level signal from the amplitude detector and the Window Open signal from the window generator must be active to enable the window logic. The Level signal is active provided the amplitude of the signal presently passing through the decoder PCA has exceeded either the positive or negative threshold established by the threshold generator and threshold comparator (whether in a slave or the master tape unit) or if it has been less than three DF periods since the last threshold-exceeding bit.

The Window Open signal is clamped in the inactive condition (and the Window Closed signal is clamped in the active condition) until the Enable Window Logic (EWL) signal from the state control logic becomes active.

In read-only mode, the EWL signal becomes active only after the state control logic is satisfied. The state logic is satisfied when at least one channel is active for 20 consecutive DF periods and the Identification Burst (IDB) and Tape Mark (TM) sig-

nals are inactive. (If IDB or TM are active, EWL is unnecessary since IDB or TM do not pass through the data processing circuits).

In read-after-write mode, the EWL signal becomes active under conditions similar to those in read-only mode except that the state control logic requires that at least one Level signal be active during every DF period for only five (instead of 20) DF periods. (However, after this test, all nine Level signals must be active for the next 20 consecutive DF periods before the input signals will be recognized as valid).

These precautions provide reasonable assurance that the block being read is not noise and that it is a valid block. The EWL signal becomes active after the first twenty (read-only mode) or the first five (read-after-write mode) bytes of the preamble of the data block. The first 40 bytes of the preamble are all zeros.

The window generator is hard wired to preset to count 05(0101). Each time a data bit is transferred from the level change register to the skew buffer, it goes through the window logic and a preset signal is generated. Since the generator is a decade counter followed by a binary counter a 40 DF signal is used as a clock each count 05, 06, 07, 08, 09 is equal to 10 DF. (The count 09 is used only when necessary to allow data through window). At the end of count 07 the window is open for count 08 or 25% of one DF time. Another count (09) is allowed to be sure data has passed through the window. This data going through the window resets the window generator to count 05. The 3 counts 05, 06, 07 that the window is closed corresponds to 75% of one DF time. The phase correction signal takes place at approximately the 50% time of one DF. Since the window is off for 75% of one Data Time the correction pulses do not go through the window.

After the EWL signal becomes active, arrival of the next level change in the level change register causes the window logic to preset the window generator to its initial state. After 3/4 of a DF period, the Window Open signal becomes active and enables the window logic.

With the window logic enabled, arrival of the next level change in the level change register causes the window logic to momentarily activate the Shift pulse to both the data and pointer registers of the skew buffer. This pulse is required to enter new bits and shift bits from preceding bytes in the skew buffer data register and to shift the pointer in the pointer register of the skew buffer.

However, the skew buffer takes no significant action because the pointer register has not yet been enabled by the pointer register enable latch. The Enable signal from the pointer register enable latch to the pointer register requires two conditions to become active; the EWL signal to the pointer register enable latch must be active and the pointer register enable latch must sense the presence of a logic 1 in the incoming signals. Since the first logic 1 in a data block occurs as the last (41st) bit of the preamble. With the Enable signal active, the skew buffer is ready to operate on the next bit to arrive. (This will be the first data bit of the data section of the data block). Once enabled, the Enable signal remains so until the EWL signal becomes inactive (during the postamble).

4-25. Skew Buffer Operation. Some explanation of the operation of the skew buffer is required before proceeding with the flow of data through the data circuits.

The skew buffers compensate for skew. The buffer consists of a data register, a pointer register, and a comparator. The data and pointer registers have four bit positions. When the skew buffer is enabled by the Enable signal, the next level change to arrive in the level change register is stored in the first (QA) position of the data register by the active Shift pulse from the window logic. If skew exists, some of the data bits for a given byte will arrive at the skew buffers in their channels before the last bit (which completes the byte) arrives at the skew buffer in its channel. The skew buffer in each channel keeps track of the earliest-arrived data bit which has not yet been matched, in all other eight channels to form a complete byte. It can keep track of an unmatched data bit for up to four byte times before an error signal is produced. (Figure 4-14).

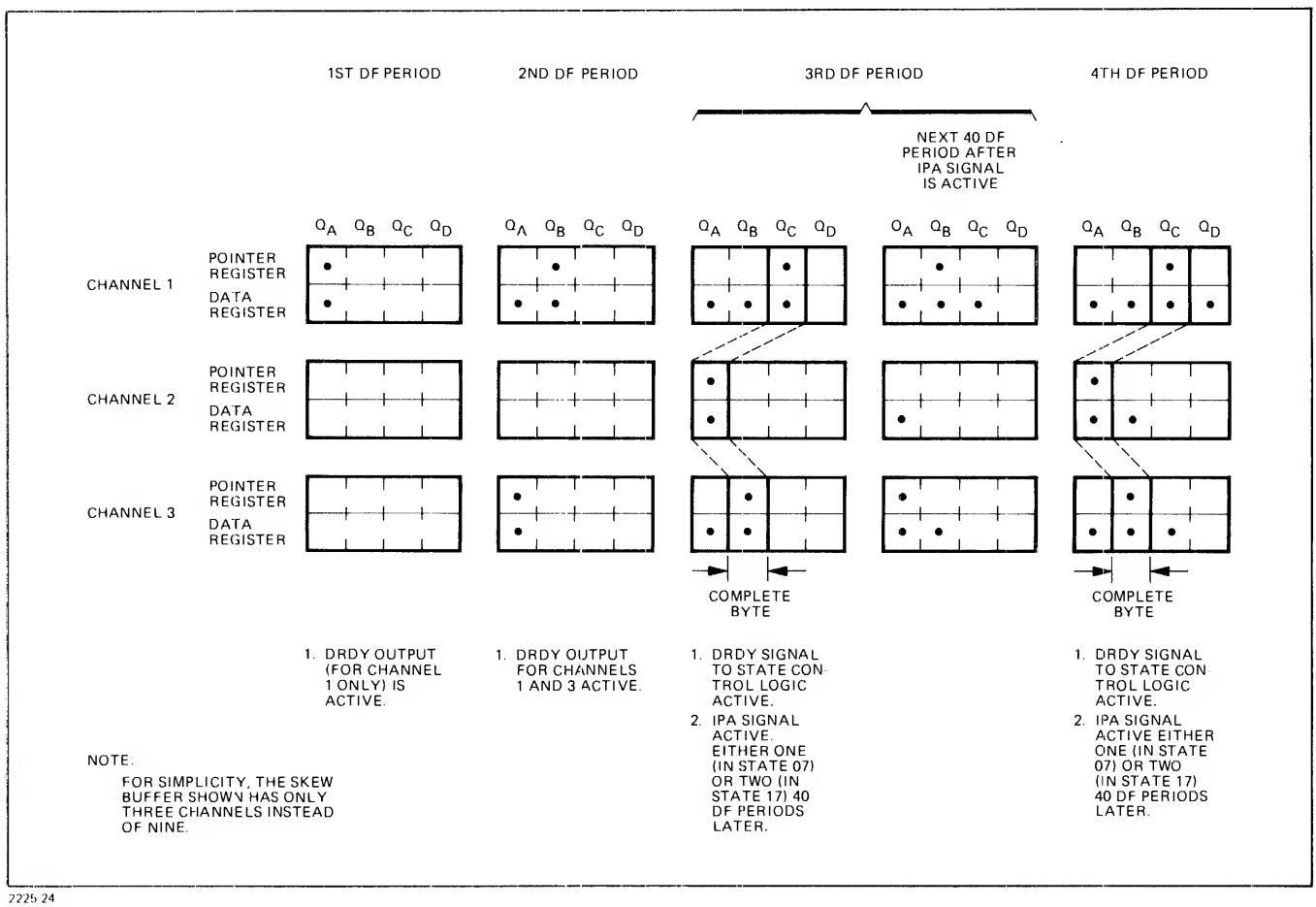


Figure 4-14. Skew Buffer Operation

The same active Shift pulse used in the skew buffer causes a pointer to be stored in the QA position of the pointer register to match the bit in the data register. The pointer register can contain only one pointer at a time. The Data Ready (DRDY) signal for a channel is activated whenever the pointer register contains a pointer. (It is also activated, under error conditions, by the error detection circuits). Presence of a pointer in the pointer register of a channel indicates that the channel has a bit ready to be transferred to the error-correction register on the data and status PCA.

If another bit arrives in the same channel before the data register in every channel contains a bit, the earliest arrived bit will be shifted one step right by the Shift signal from the window logic. The pointer, also, will be shifted one step right to continue to point at the earliest-arrived bit. As many as four bits can be stored in the data register of the skew buffer. However, if the earliest-arrived bit is not matched with bits from the other eight channesl to form a complete byte before arrival of the fifth bit in the level change register, the error detection circuits will produce an active Track in Error (TIE) signal. This is called skew buffer overflow condition.

4-26. Signal Flow (Error-Correction Register to Interface). When the data bits of the first byte of the data section of the data block enter the skew buffers, the skew buffers operate as described in paragraph 4-25 to match the data bits into a complete byte. When the earliest-arrived data bit in each channel has been matched with data bits from all other channels to form a complete byte, the state control logic is notified, through the Data Ready (DRDY) signal. The state control logic responds by storing the byte present in the error-correction logic into the output register (Output Register Storage Enable Signal), storing the data bits present in the skew buffers in the error-correction register (Error Correction Storage Enable Signal), shifting the pointers in the skew buffers to the next earliest-arrived-but-as-yet-unmatched data bits (Increment Pointer Address Signal, shift left), then clocking the byte now stored in the output register into the interface (Read Clock signal). If at the time the pointer is shifted left a channel happens to have a data bit stored in the dual change register, the pointer does not change position, but the data is clocked forward one bit. This keeps the pointer at the proper data bit.

While the byte is present in the error-correction register, the parity checker checks it for parity errors and notifies the error-correction circuits of the result (Agreement signal). The error-correction circuits also receive notice from the track-in-error (TIE) decoder logic if only one channel contains an erroneous data bit (Single-Track Error Signal). If only one track is in error it will correct the error before the byte is stored in the output register.

If the error-correction circuits receive notice from the parity checker that a lack of parity exists in the byte stored in the error-correction register, yet the El signal from the TIE decoder logic doesn't indicate a single track error, the error correction circuits notify the state control logic (Even signal). The state control logic then notifies the interface that errors exist in the data block being read (Multiple Track Error Signal) and reading of the data block is discontinued. The remaining data in the block will be passed over.

4-27. Postamble Events. The PE read circuits continue to operate, as described, on all bytes of the data section of the data block until the postamble occurs. The skew buffer output sensing circuits and the end of data logic together sense the presence of the first byte of the postamble in the error-correction register. When this condition exists, the end of data logic informs the state control logic (through the End of Data signal) so that it will know the data section of the data block is complete. The skew buffer output sensing circuits maintain a steadily active Skew Buffers Equal Zero Signal (SBEZ) to the state control logic while the postamble (from the second byte to the forty-first byte) is passing through the nine skew buffers. This is used by the state control logic, in read-after-write mode (and, under certain conditions, in read-only mode) to ensure that the postamble is properly written.

When the state control logic is informed by the End of Data (EOD) signal that the data section of the data block has been read, it deactivates the EWL signal to inhibit passage of signals through the data circuits on the decoder PCA's. In read-only mode, this occurs at the beginning of the postamble. However, in read-after-write mode and in read-only mode when a single track error exists while the EOD signal is active, the EWL signal remains active until the thirty-sixth byte of the postamble. This keeps the data circuits on the decoder PCA's enabled until near the end of the postamble to check the greater part of the postamble for errors.

In read-only mode, twenty DF periods after the last byte of the postamble has passed the tape heads, (some of the circuits on the decoder PCA's, including the low amplitude detector, are still active since they do not require an active EWL signal to operate), the state control logic and output logic generate the End of Block (EOB) signal to the interface. At the same time, the state control logic clears the error-correction and output registers on the data and status PCA and prepares its associated circuits (state control counter and state flip-flops) for the next information block.

4-28. Error Detection. The error detection circuits on the decoder PCA check for four types of errors (discussed later). If any one of these errors occur, the error detection circuits indicate to the TIE decoder logic (Track in Error Signal), on the data and status PCA, that the channel in which the error detection circuits are located is in error. They also activate the DRDY signal from the channel in which an error has been detected. Thus, if all the other eight channels have an active DRDY signal (indicating they either have a data bit to contribute to complete the byte or they have an error), the state control logic is notified, just as though nine data bits have been matched to form a complete byte. The state control logic learns later, through signals from the TIE decoder logic (Single-Track Error and More Than One TIE signals), of the error status of the byte.

The TIE decoder logic, on the data and status PCA, receives the error status indications from all nine channels. It notifies the error-correction circuits and state control logic whether or not: no channels contain errors, only one channel contains an error, or more than one channel contain an error (Single-Track Error and More Than One TIE signals). If no channel contains an error, no action is taken. If only one channel contains an error, it is corrected by the error-correction circuits and the state control logic and output logic informs the interface (through the Single-Track Error signal) that a single channel error has occurred

(even though it has been corrected). If more than one channel contains errors, the state control logic and output logic so inform the interface (Multiple Track Error signal) and the state control logic causes the remainder of the block to be passed over without being read. Then the PE read circuits prepare to read the next block.

4-29. PE NRZI Write Circuits. The following paragraphs contain a functional description of the PE write circuits on a block diagram level and a detailed discussion of each circuit.

The write circuits are similar for both PE and NRZI. They are contained on seven PCA's; the write control PCA, five write data PCA's and the write motherboard PCA. Four of the five write data PCA's contain two write channels each. The fifth write data PCA contains a single channel. The write motherboard PCA contains the wiring which interconnects the write PCA's and interfaces between the write circuits and external circuits.

The write circuits (figure 4-15) consist of the write control circuits, the +5V sense circuit, the data circuits, the clock circuits, the erase circuit, and the write reset circuit. However, the write reset circuit is used in NRZI formats only.

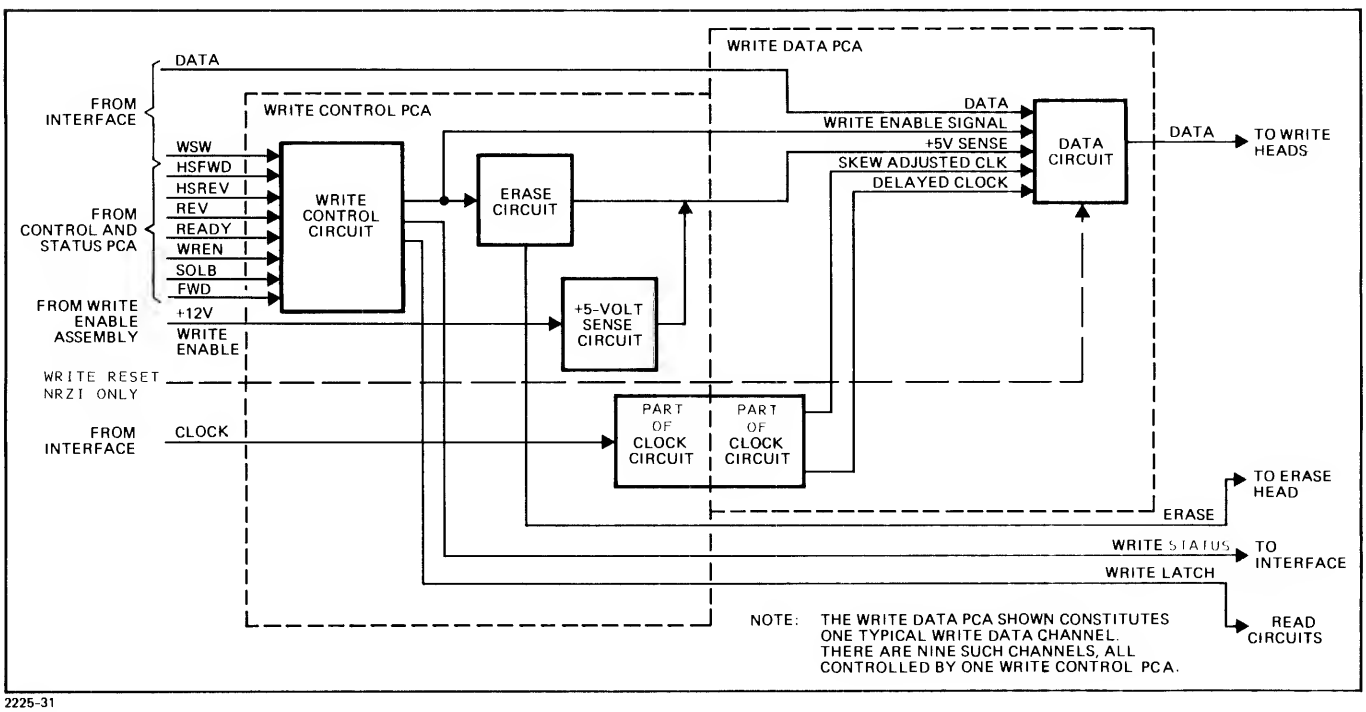


Figure 4-15. PE/NRZI Write Circuits, Block Diagram

A tape reel equipped with a write enable ring will cause the write enable solenoid to energize. With the solenoid energized +12 volts (+12 WE) is provided for the write circuits.

The write control circuits, when activated by eight input signals, enable the data circuits to enable writing. They also enable the erase circuit and generate the Write Latch signal to the read circuits and the Write Status signal to the interface. These two signals are status signals which indicate whether or not the write circuits are in write mode.

The data circuits, when enabled by signals from the write control and write enable circuits, digitize and skew compensate the data signal and supply it to the write heads.

The clock circuits consist of the clock delay circuit and the Skew Adjustment one-shot multivibrator. The clock delay circuit delays the clock pulse train to ensure that the data bit on the data line has settled to a steady state before it is stored in the data circuits. For PE write only, the PE clock from the interface is at twice data frequency (for phase correction pulses).

The Skew Adjustment one-shot enables delay of the data stream in the channel in which it is located so that the data bits will be written at the same time as the data bits in the channel with the greatest time lag (due to skew). Thus, with the proper adjustment of the Skew Adjustment one-shot in each channel, the data bits for all channels will be written at the time required to correct for write head static skew.

The erase circuit, when enabled by inputs from the write control circuits and the write enable circuit, cause the erase heads to erase the tape before it is supplied to the write heads. The +5 volt sense circuit senses the 12 volt enable voltage (WE) and gates +5 volt sense signal to the data circuit write amplifiers.

MAINTENANCE AND TROUBLESHOOTING

SECTION V

5-1. INTRODUCTION.

This section contains a list of test equipment needed to perform maintenance on the tape unit, procedures for preventive maintenance, checkout procedures, performance tests, adjustment procedures, and troubleshooting procedures.

5-2. TEST EQUIPMENT.

The test equipment required to perform maintenance and troubleshooting on the 7970B/7970E Tape Unit will supply input commands to simulate the commands normally received from the interface, and supply visual indications of the tape unit output signals normally sent to the interface. These requirements can be met by a computer and interface or by the following test PCA's available as accessories to the tape unit. Procedures in this maintenance section are written assuming use of the test PCA's.

5-3. TEST EQUIPMENT REQUIRED.

Listed below is all equipment needed to perform all maintenance on the tape unit.

CAUTION

Do not use NRZI and PE reference amplitude test tapes 5080-4547 and 5080-4548 on read/write units. Use of these tapes on read/write units can cause degradation of tape signal strength because of residual erasure.

a. Write test PCA, 13192-60010.
b. Write programmable PCA, 13192-60020.
c. Control and status test PCA, 13191-60010.
d. Master alignment tape, 9162-0027.
e. Test tape, standard speed, 5081-9401.
f. Amplitude reference tape, 5080-4548.
g. Test tape, PE read circuits, 5080-4555.
h. Write formatter PCA, 13195-60000.
i. Write formatter test PCA, 13196-60001.
j. Read data PCA, 13196-60000.
k. Extender board kit, 07970-62114 (PE Read-Only).
l. Extender board, 07970-60420 (7970B only).
m. Both k and l above (7970E Read/Write, Read-Only dual or triple format).

n. Any good quality scratch tape certified 3200 frpi or better.

o. HP 180 oscilloscope, dual trace or equivalent.

p. HP 5306A multimeter/counter or equivalent.

NOTE: The read data test PCA is needed to perform maintenance on the PE read circuits. The write formatter PCA and write formatter test PCA are needed to perform maintenance on the write circuits. The control and status test PCA is needed for maintenance on all circuits, including the transport and NRZI circuits. The NRZI read test board accessory is needed for maintenance on the NRZI circuits only. As an example of hookup configuration, figures 5-1 and 5-2 illustrate connection of the test PCA's to a master tape unit.

5-4. PREVENTIVE MAINTENANCE.

Preventive maintenance information for the HP 7970 tape units consist of fuse replacement information and five types of inspection, cleaning, and test procedures to be performed after 8, 500, 1000, 2000, and 5000 hours of tape unit operation time.

5-5. FUSE REPLACEMENT.

Fuses used in the tape unit are ac line fuses and secondary voltage fuses.

5-6. AC LINES FUSES. The two ac line fuses are located on the interior, rear panel. For 115 Vac operation, a 4 ATT fuse is required (TT: super time lag). For 230 Vac operation, a 2.5 ATT fuse is required.

5-7. SECONDARY VOLTAGE FUSES. The secondary voltage fuses are mounted to the power supply PCA. Fuse values are placarded at or near the fuse holder.

5-8. EIGHT-HOUR PROCEDURE.

To perform the eight-hour preventive maintenance procedure, proceed as follows:

a. Run tape and visually check for tape scraping on reel flanges, tape guide flanges, or uneven travel on the capstan. If tape reel flange scraping is observed, verify that the reel is properly seated on the hub.

b. Remove tape reels.

c. Set power switch to OFF.

d. Push head gate (crosstalk shield, installed on read/write units) inward and hold to clean read/write heads.

NOTE: Clean tape path components with cotton tipped applicators (HP part number 8520-0023, or equivalent) and lint-free wipers moistened with one of the cleaners listed below. Use cleaners sparingly and avoid contaminating bearings. Be alert to any mechanical malfunction to prevent possible damage to recorded data.

(1) Head Cleaner (HP 8500-1251).

(2) Genesolve D (Allied Chemical).

(3) Freon TF (Dupont).

e. Clean the heads and check for scratches.

f. Release head gate to operating position (read/write units only).

g. Clean the tape cleaner.

h. Clean the photosense head.

i. Clean the stationary guides and rollers. Verify that moving rollers are revolving freely.

j. Clean the capstan. (Use solvents on rubber capstan sparingly).

k. Clean the transport area.

NOTE: Cover door is fitted with plexiglas. Brush away any heavy residue with a soft-bristle brush and clean gently with a wiper and commercial glass cleaner. Ensure that the reel holddown knob is seated to prevent scratching the plexiglass.

l. Set power switch to ON.

m. Install tape reels.

n. Thread tape.

o. Tension tape and position at loadpoint.

p. Make density selection.

q. Make unit address selection.

r. Place unit on-line.

5-9. 500-HOUR PROCEDURE.

To perform the 500-hour preventive maintenance procedure, proceed as follows (refer to Performance Tests):

a. Clean tape transport.

b. Check reel hold-down assembly.

c. Check photosense head assembly.

d. Check write enable assembly.

e. Check regulated power supply.

f. Check capstan servo.

(1) Off-set adjustment.

(2) Tape speed.

(3) Start-stop ramp.

g. Check positions of tape tension arms.

h. Check all tape motion functions.

5-10. 1000-HOUR PROCEDURE.

To perform the 1000-hour preventive maintenance procedure, proceed as follows (refer to Performance Tests):

a. Perform 500-hour checks.

b. Check tension arm photosense.

c. Do performance test on entire tape unit (refer to paragraph 5-76).

5-11. 2000-HOUR PROCEDURE.

To perform the 2000-hour preventive maintenance procedure, proceed as follows:

a. Perform 500- and 1000-hour checks.

b. Replace photosense assembly lamp.

c. Replace tension arm assembly lamp.

5-12. 5000-HOUR PROCEDURE.

To perform 5000-hour preventive maintenance procedure, proceed as follows:

a. Perform 500-, 1000-, and 2000-hour checks.

b. Replace tape roller assemblies.

c. Replace capstan pulley assembly.

5-13. 7970B/7970E ALIGNMENT AND PERFORMANCE ADJUSTMENTS.

5-14. TEST EQUIPMENT REQUIRED.

The following test equipment or equivalent is required to perform the adjustments.

a. A means of dynamically operating the tape unit at drive rates specified in the procedure. The 13191A Control and Status Test Board is available as a service accessory and will meet the needs of all adjustments. Computer operation is also suitable.

b. HP 180A Oscilloscope, or equivalent.

c. HP 5245L Counter, or equivalent.

d. Digital Volt Meter.

e. IBM Master Skew Tape HP part number 9162-0027.

f. Transport Test Tape 5080-4525, 2400 foot tape, or 5081-9401, 1200 feet. (7tr used in both 7tr and 9tr alignment).

g. Scratch Tape.

5-15. MECHANICAL ADJUSTMENTS.

Transport mechanical adjustments consist of tape roller, tension arm, tension arm limit switch, write enable switch, and reel retaining knob adjustments.

5-16. TAPE ROLLER. All tape rollers are precision referenced to the step in the shaft on which they are mounted. Under no circumstances should any adjusting shims be placed between the inner bearing and this step. Shimming is done at the outer end of the roller. Assembly should consist of one shim next to the bearing then the preload washer, followed by shims to remove all end play. Proper preload will exist when there is one shim beyond the number required to just remove the end play. Shim thickness is 0.005 inch nominal.

a. Ensure that brass nut (figure 5-1, item 7) is torqued to 5 inch pounds.

b. Install assembly components as indicated in figure 5-1. Use retaining Ring Pliers (Walder 18-23; Industrial Retaining Ring Corp. P100; or equivalent). Avoid distorting retaining ring.

c. Check tape roller bearing assembly (6) for end-play. Add/remove flat washers (3 or 2) until end-play is just removed.

d. Spin bearing assembly and check for drag. The tape roller must spin freely. If the tape roller does not spin freely loading is excessive; recheck end-play clearance.

5-17. TENSION ARM. The tension arm adjustments consist of:

a. Properly positioning the photosense mask (shade) and the tension arm such that; the zero error (Null) voltage reference, in the reel servo loop, occurs near the midpoint of the tension arm's arc.

b. Ensuring that the maximum deflection of the tension arms is symmetrical with respect to the maximum points marked on the casting.

c. Positioning the limit switches relative to the tension arm.

Static Tension Arm Adjustment.

NOTE: This adjustment is made at the factory. If replacement of either tension arm assembly is required in the field this procedure must be performed before the remaining electro-mechanical adjustments.

a. Ensure that a minimum clearance of 0.010 inch exists between the Cell and the outer side of each photosense mask; use a feeler gauge.

b. Remove the supply and take-up reels from the unit and slightly loosen the allen screw holding the supply reel photosense mask.

c. Hold the upper tension arm in the center, indicated by the two drilled holes on the back of the door casting and press the LOAD pushbutton on control switch panel.

d. Adjust the mask to eliminate supply reel motor motion and tighten the allen screw.

NOTE: Watch back of motor for shaft rotation.

e. Place a non-metal pencil through the casting slot for the upper tension arm.

NOTE: This prevents the tension arm from tripping the upper limit switch, thus de-energizing reel servo circuits.

f. Loosen the allen screw holding the lower tension arm mask and hold the tension arm in the center position.

g. Press LOAD if necessary and adjust the photosense mask to eliminate lower reel motor motion.

h. Tighten the photosense mask socket screw.

i. Remove the pencil and mount a scratch tape, press and hold LOAD pushbutton and observe tape tension adjustment. There should be no reel rotation and the tape should be tensioned with tension arms at their midpoints.

5-18. TENSION ARM LIMIT SWITCHES. The limit switch mounting bracket pivots on the screw that mounts the tension arm rubber stop. The hole for the adjacent screw is elongated to provide limit switch positioning adjustment; this screw locks the mounting bracket in position after completion of the adjustment. Mounting holes for the microswitch are also elongated, providing slight additional limit switch adjustment movement. To position the limit switch, rotate the bracket and/or adjust height position to achieve the following conditions:

a. When arm is fully against bumper, the roller on the microswitch should be approximately at the high point of the arm diameter without being over center.

b. Pull the tension arm down and away from the bumper 1-2 inches. As the tension arm is allowed to slowly return to the stop, the microswitch must operate within 1/8 inch of the bumper. As the tension arm continues its travel to the bumper, the actuating arm of the microswitch must also continue to travel. (It must not bind against the switch body).

c. Verify that all screws are tight prior to final confirmation of "a" and "b". Repeat adjustment for all three limit switches. If background noise permits, switch operation can be checked audibly; otherwise connect a suitable ohmmeter across the switch terminals. If ohmmeter is used, verify that power is not applied to the tape unit.

5-19. WRITE ENABLE SWITCH. The write enable switch must be positioned to ensure clearance when operated with a tape reel that does not have the write enable ring installed (tape is file protected) and to ensure both retraction and operating clearance when used with a reel that has the write enable ring installed. These conditions will be established when the proper dimensional relationships exist between the write enable sensing finger and the outer face of the reel turntable. To obtain these required dimensional relationships, perform the adjustment procedure in the order indicated. (See figure 5-2).

a. Loosen switch S1 mounting screws.

b. Manually place the sensing finger even with the edge of the turntable. With power removed, adjust the position of S1 until an audible click indicates that switch S1 is closed.

c. Tighten switch S1 mounting screws.

d. Apply power and manually place the sensing finger even with the turntable. Verify that the solenoid energizes and completely retracts the sensing finger.

e. Adjust the reel turntable flange diameter clearance as follows:

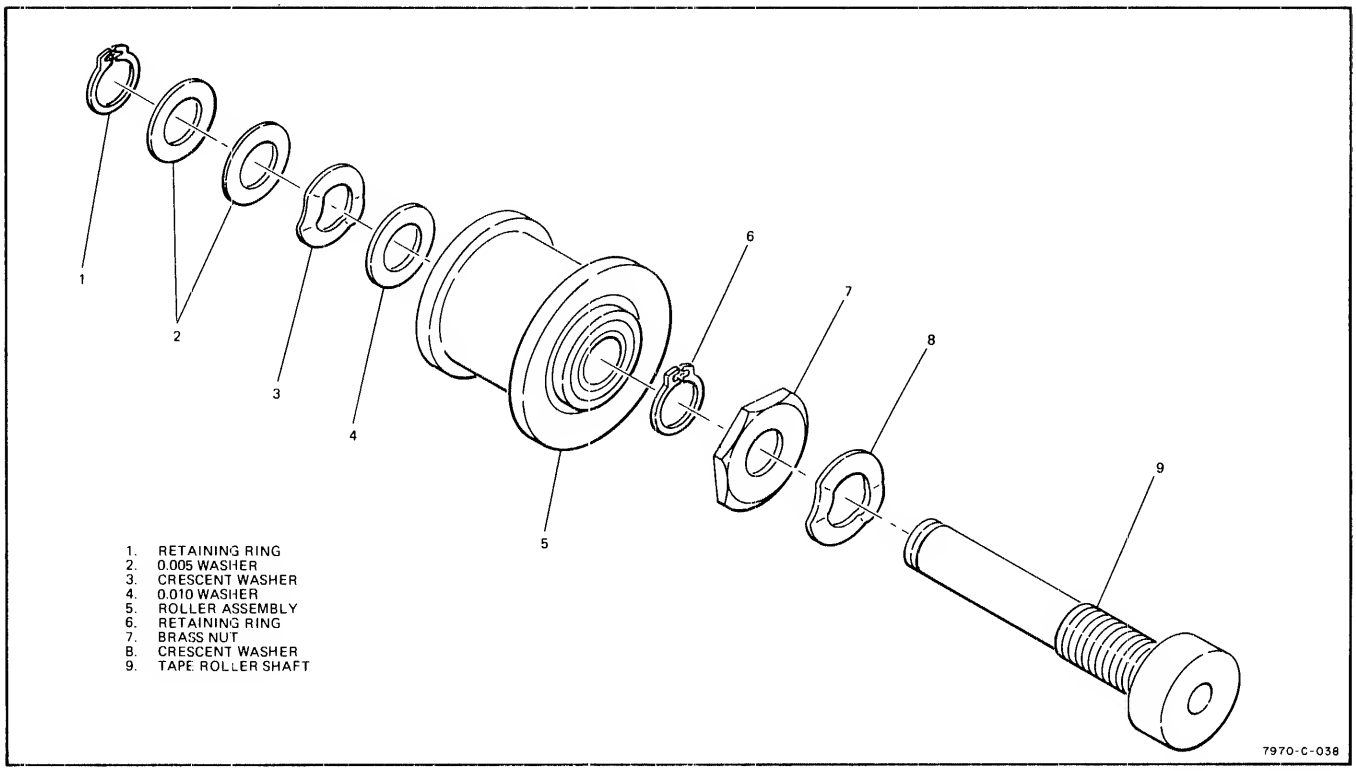


Figure 5-1. Tape Roller Assembly

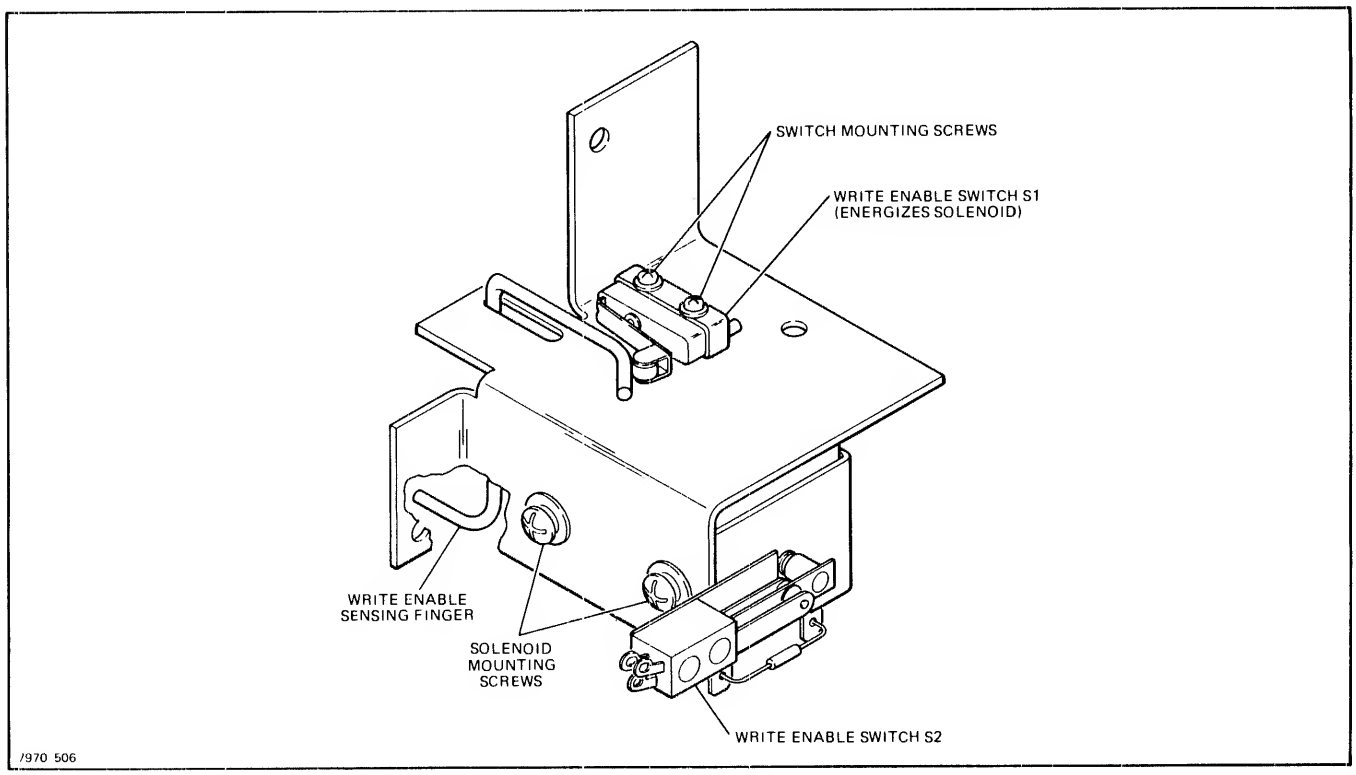


Figure 5-2. Write Enable Assembly

1) Loosen write enable assembly mounting screws.

2) Position the write enable assembly So that the sensing finger will clear the reel flange diameter throughout solenoid travel.

3) Tighten write enable assembly mounting screws.

5-20. REEL RETAINING KNOB. This adjustment is made during manufacture but may require some correction during the life of the tape unit. When the locking lever is working properly, it should be possible to place the reel over the rubber with a minimum of interference. When the locking lever is closed, positive resistance should be encountered as the rubber is compressed. In the locked position, it should not be possible to move the reel, (with respect to the hub) by hand. If slippage is suspected, place a piece of masking tape on the reel, another on the hub. A mark placed in alignment on both pieces of tape should not become misaligned by more than 1/8 inch in 16 hours of operation. To correct tape reel slippage, release locking lever and loosen the pozidrive screw, rotate the reel retainer knob clockwise, and tighten screw. Repeat until tape reel mounts firmly and does not slip. The tip of the screw fits into notches of the turntable. If the screw does not seat all the way down, back off and move the hub on the turntable a slight amount and retighten screw.

5-21. ELECTRICAL ADJUSTMENTS.

The electrical adjustments of the tape unit are very critical and must be performed in the following sequence.

a. Power supply adjustments.

b. Capstan motor offset current adjustment.

c. Capstan servo forward and reverse drive speed adjustments.

d. Capstan servo high-speed forward adjustment.

e. Capstan servo high-speed reverse adjustment.

f. Capstan servo ramp slope adjustment.

g. Reel servo adjustments.

5-22. POWER SUPPLY ADJUSTMENTS. Only one adjustment is provided for the three regulated supplies. The adjustment control is located in the circuitry for the +12-volt supply but is adjusted to establish the value of the +5-volt supply, which is held to a tighter operating tolerance. The value of the +12 and -12 volt supplies is established by a precision resistor network. The adjustment control, +5V, +12V, and -12V test points are located on the power regulator printed circuit assembly. Voltage is correctly adjusted when the following conditions are met:

a. +5 ± 0.050 Vdc. (Adjust to + 0.010 Vdc when adjustment is required).

b. +12 ± 0.360 Vdc.

c. -12 ± 0.360 Vdc.

NOTE: Final reel servo adjustments must be made after the capstan servo adjustments. The capstan speed must be within tolerance in order to properly adjust the reel servo adjustments. If the tape unit does not maintain tension, perform the reel servo adjustments initially, complete the capstan servo adjustments, and repeat the reel servo adjustments.

5-23. CAPSTAN MOTOR OFFSET CURRENT ADJUSTMENT. Prior to making the capstan motor offset current adjustment, verify that the power supply voltages have been adjusted.

For capstan switch and adjustment locations see figure 5-3.

Connect a suitable dc voltmeter (capable of resolution to ±5 mv dc) across the 3-ohm resistor (R21 or R22) connected in series with the capstan motor. The common side of the resistance is associated with pin 2 of CJ1 and the high or motor side is associated with pin 2 of CJ2.

Load the tape transport and be sure the tape is stopped. Adjust OFFSET control until voltmeter reading is minimum. An acceptable minimum is any value which is between ±0.100 Vdc. Typical adjustment at room ambient temperature (25°C) will be in the order of ± 0.080 Vdc.

5-24. CAPSTAN SERVO FORWARD AND REVERSE DRIVE SPEED ADJUSTMENTS. Prior to performing the servo forward and reverse drive speed adjustment, ensure that power supply voltages and offset current are within tolerance. Figure 5-3 shows the location of service switches and forward and reverse speed adjustments used in the next step.

Accurate adjustment is based on reading (into a counter) data bits that have been recorded with high average accuracy. The 5080-4525 and 5081-9401 Test Tapes have bit-to-bit accuracy of better than 0.1 percent when measured over 2000 bits or more. In using this tape, it is important to recognize that there are two data bits for each cycle counted when the counter is connected to the preamplifier analog output signal. Also the frequency at other than the specified tape speeds may be calculated on a direct ratio basis.

a. Load test tape (5080-4525 and 5081-9401) and place unit in forward drive mode using FWD service switch (S2).

b. The test tape provides a signal of 10,000 Hz at a tape speed of 30 ips and has a bit-to-bit distance of 0.0015 inch.

c. The signal used for the following adjustments appears in preamplifier channel 3 of nine-track units and preamplifier channel 6 of seven-track units.

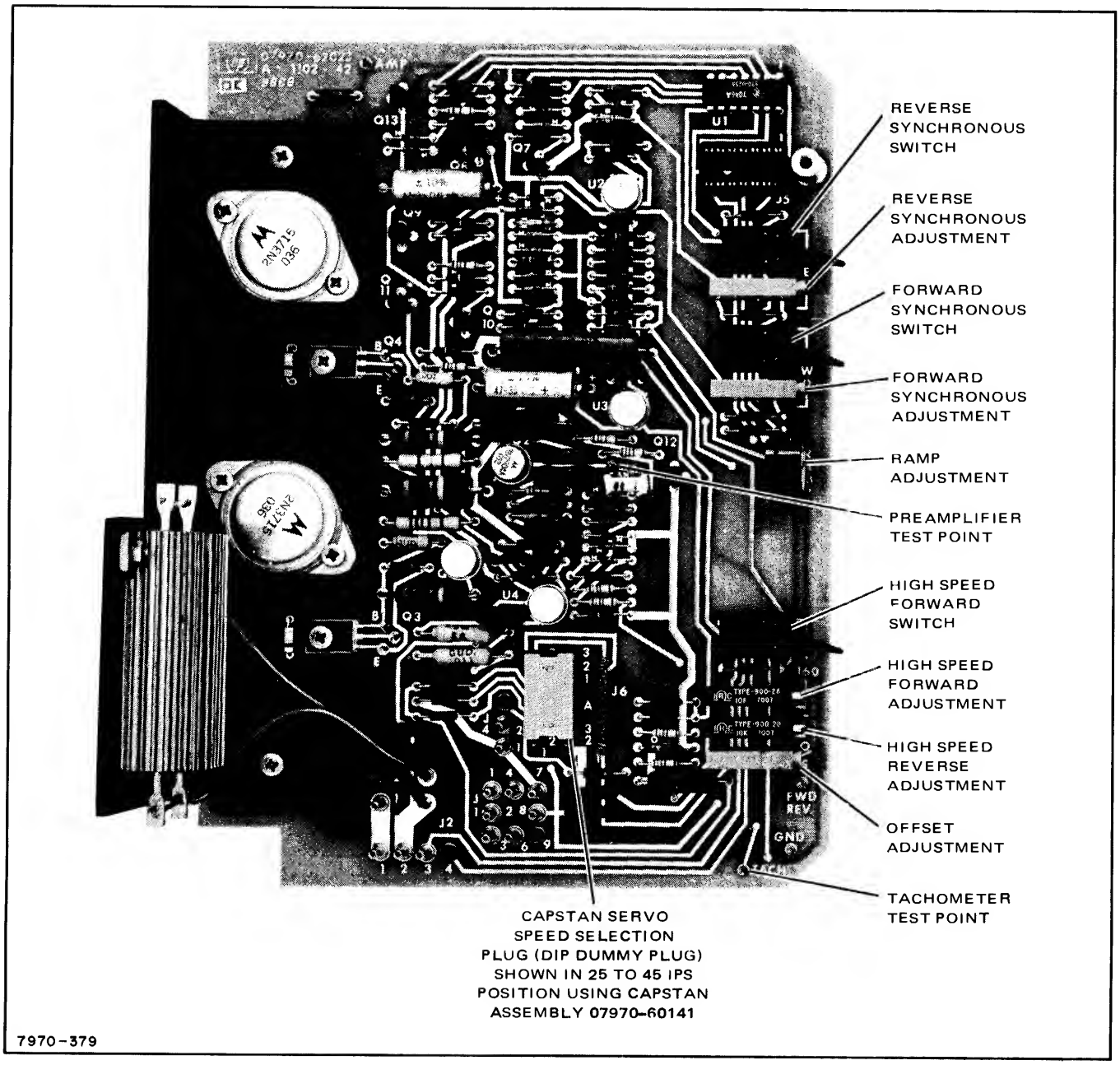


Figure 5-3. Single Speed Capstan Servo PC Assembly, Test Points and Adjustments

d. Adjust the FWD synchronous control (R34) if necessary, until counter indication is as follows:

(1) For 25 ips speeds, the counter indication should be 8,333 ± 34 Hz. If adjustment is necessary, adjust to 8,333 ± 16 Hz.

(2) For 37.5 ips speed units, the counter indication should be 12,500 ± 50 Hz. If adjustment is necessary, adjust to 12,500 ± 25 Hz.

(3) For 45 ips speed units, the counter indication should be 15,000 ± 60 Hz. If adjustment is necessary, adjust to 15,000 ± 30 Hz.

e. Repeat steps "a", "b", "c", and "d" with unit in reverse drive mode.

5-25. CAPSTAN SERVO HIGH-SPEED FORWARD ADJUSTMENT. The high-speed forward adjustment principles and requirements are the same as the forward and reverse drive adjustment. Ensure that all previous adjustments are within tolerance.

a. Load the test tape on the transport and connect a counter to the appropriate channel preamplifier output.

b. On the capstan servo PCA place unit in high-speed forward mode with the high-speed forward (+160) service switch (figure 5-3), and use the high-speed forward (+160) adjustment (R53) to adjust speed until counter indicates 53,333 ± 800 Hz. If adjustment is required, adjust until the counter indicates between 53,233 and 53,433.

c. If unit requires high speed other than 160 ips, the frequency indication of the counter should be (333.3) x (speed).

5-26. CAPSTAN SERVO HIGH-SPEED REVERSE ADJUSTMENT. The high-speed reverse adjustment is identical the the high-speed forward adjustment, except that the control switch (front of tape drive) REWIND pushbutton is used to place the unit in the high-speed reverse mode and the high-speed reverse (-160) variable resistor (R60) is used.

5-27. ALTERNATE METHOD FOR CAPSTAN SERVO ADJUSTMENT.

NOTE: This method is to be used only if a transport test tape and a frequency counter are not available. This method further increases the tolerance and should be used ONLY when proper equipment is not available and the situation is critical.

a. Equipment needed, master skew tape (9162-0027) and Oscilloscope HP model 180 or equivalent.

b. Calculate the data clock period using the following formula:

$$\text{Period} = \frac{1}{\text{Density} \times \text{Speed}}$$

Example: Skew tape 9162-0027 is recorded at 800 BPI and assume 45 ips.

$$\text{Period} = \frac{1}{800 \times 45} = \frac{1}{36K} = 28 \text{ micro secs.} = \text{data clock.}$$

c. Install master skew tape and connect the oscilloscope to the read clock (RC) test point on the read control PCA.

CAUTION

Do not, at any time, perform a high speed operation with the Master Skew tape loaded on transport. High speed operation tends to stretch the tape and destroys its accuracy. Use the REV service switch (S1, capstan servo PCA) to rewind the tape.

d. Place the tape unit in forward drive mode by using FWD service switch (S2) located on the capstan servo PCA.

e. Adjust the FWD potentiometer on the capstan servo PCA for the clock period calculated in step 2. Stop transport.

f. Place tape unit in reverse drive mode by using REV service switch (S1) located on the capstan servo PCA.

g. Adjust the REV potentiometer on the capstan servo PCA for the clock period calculated in step 2. Allow tape to completely return to the supply reel.

5-28. CAPSTAN SERVO RAMP SLOPE ADJUSTMENT, SINGLE SPEED. The ramp slope adjustment determines the start and stop distances for both forward and reverse drive modes. The following procedure describes how to adjust the slope of the bi-polar ramp generator on the capstan servo PC assembly. This adjustment sets the start distance to 0.1875 inch. The top of the ramp is rounded, therefore, the 90% point of the voltage waveform is used. (See figure 5-4).

a. Ensure 13191A, Control and Status Test Board, is installed and PROG-MAN (PROGRAM-MANUAL) switch is in the PROG position.

b. If a 13191A Control and Status Test Board is unavailable, some outside source for start and stop commands must be available (cpu).

c. Unit must be in the on-line status.

d. Switch the command forward (CF) switch on the 13191A board ON (up).

e. Connect an oscilloscope to the FWD/REV test point on the capstan servo PCA. Sync the oscilloscope with the negative going edge of the forward command (test point 9 of the control and status PCA).

f. Adjust the capstan servo PC assembly RAMP control (See figure 5-3) to obtain the time listed in table 5-1 for tape unit synchronous speed. Use the vertical gain vernier control of the oscilloscope to expand the waveform so that the 90%

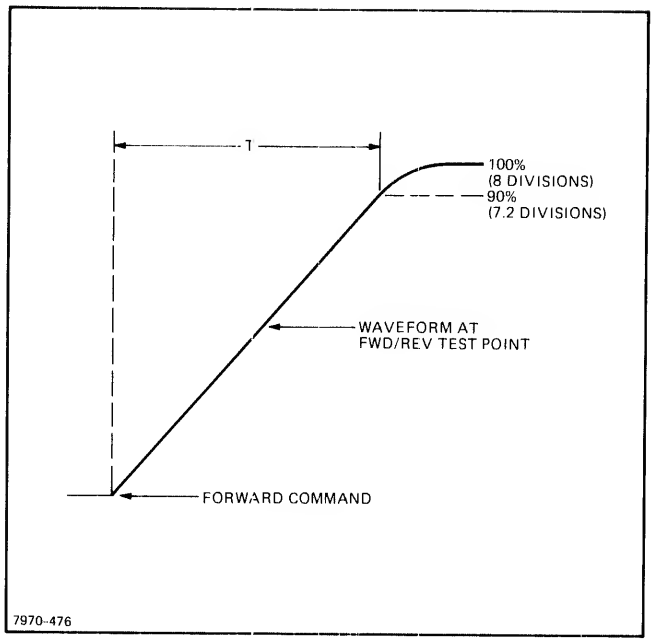


Figure 5-4. Capstan Servo Start/Stop Ramp Time

point may be conveniently measured.

NOTE: The HP 180 oscilloscope has a special horizontal time scale on the line that represents 7.2 vertical divisions. This line represents 90% of 8 vertical divisions and may be used to measure the time at the 90% voltage level for the capstan ramp adjustments.

Table 5-1. Capstan Servo Start/Stop Time

SPEED (ips)	TIME (90%)
12.5	26.1 ms ± .5 ms
18.75	17.1 ms ± .2 ms
22.5	14.1 ms ± .2 ms
25.0	12.6 ms ± .2 ms
37.5	8.1 ms ± .1 ms
45.0	6.6 ms ± .1 ms

5-29. CAPSTAN SERVO RAMP SLOPE ADJUSTMENT, DUAL SPEED. Ramp slope adjustment procedures for both synchronous speed and half-speed are identical to those for the single speed capstan servo with the following exceptions:

Synchronous speed is adjusted by variable resistor R105.

Half-speed ramp is adjusted by variable resistor R106 and the time for half-speed ramp is found in table 5-1 or the formula:

$$T = \left(\frac{.375}{\text{Speed (ips)}} - .001\right) (.9)$$

5-30. REEL SERVO ADJUSTMENTS. Load a short (200-400 foot) tape onto the transport and bring to load point. The following adjustments determine the peak deflections of the tension arms. The amount of deflection desired is a function of the synchronous speed. At 45 ips the deflection is set so the tension arms deflect to the outer marks located on the back side of the casting (in both forward and reverse modes). At lower speeds the amount of deflection is smaller (i.e. 25/45 of maximum deflection for 25 ips, or approximately 1/2 that of 45 ips). Use the drive control switch on the capstan PCA (figure 5-3) to drive the tape unit for the following adjustments.

a. With the supply reel loaded with approximately 200 feet of tape, rotate the supply reel motor variable resistor (lower) on the reel servo PCA for the deflection desired.

b. Stop tape motion, put unit in reverse drive and make sure the amount of deflection is the same as it was in forward drive (compare displacement from maximum deflection marks in casting). If not, readjust the mask position as in paragraph 5-17 until symmetrical swings are attained. (Symmetry is in respect to maximum deflection marks in casting).

c. Repeat procedure for the takeup reel with approximately 200 feet of tape on the takeup reel. (Adjust takeup reel motor variable resistor (upper) on reel servo PCA).

5-31. READ ADJUSTMENT PROCEDURES (NRZI).

The adjustment procedures for the read modules consist of preamplifier gain adjustments, forward static skew adjustments, reverse static skew adjustments, and read character gate adjustment. Ensure that all transport adjustments have been made and that all adjustments are within tolerance. Ensure 13191A (Control and Status Test PCA) and, where applicable, 13192A (Write Test PCA) are installed. See figures 5-5, 5-6, and 5-7.

5-32. PREAMPLIFIER GAIN ADJUSTMENTS. The gain/bandwidth characteristics of the preamplifier will cause small changes in phase that will affect the static skew compensation if the preamplifier gain control is adjusted. Therefore, it must be adjusted prior to the read static skew compensation, and if changed, the read static skew adjustment should be rechecked. Adjustments are made as follows:

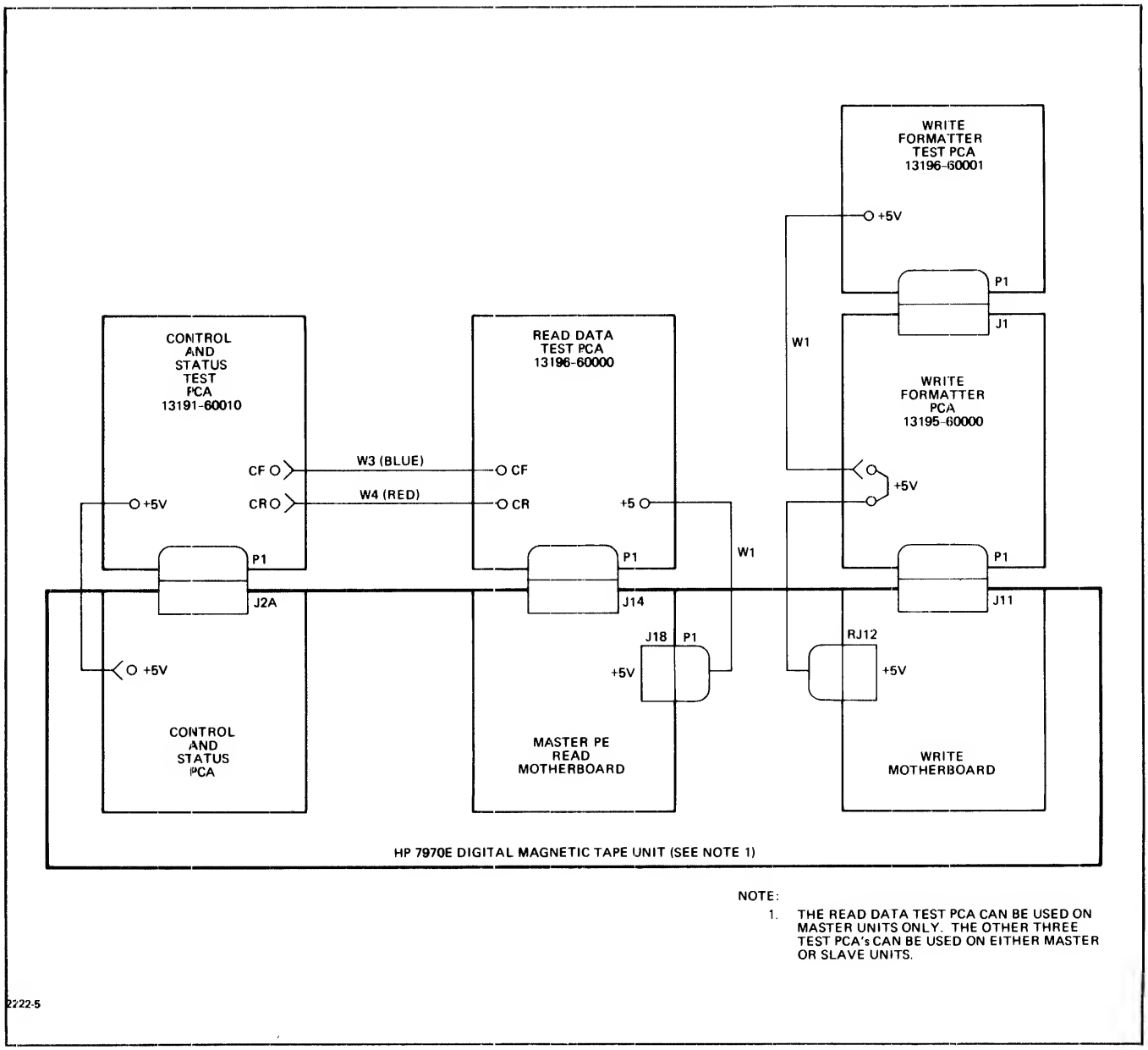


Figure 5-5. Test PCA Installation
for Testing PE Read and Write Circuits

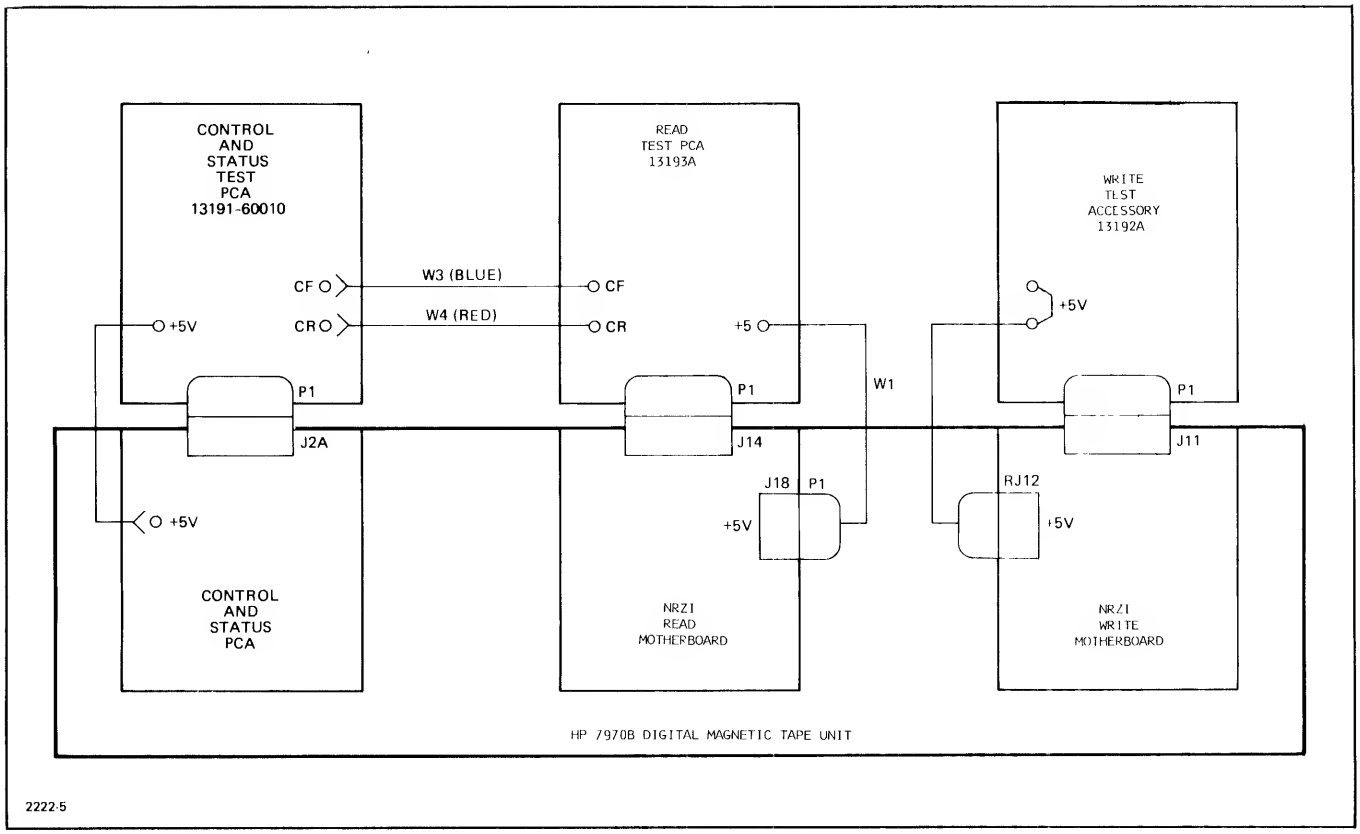


Figure 5-6. Test PCA Installation for Testing NRZI Read and Write Circuits (7970 B)

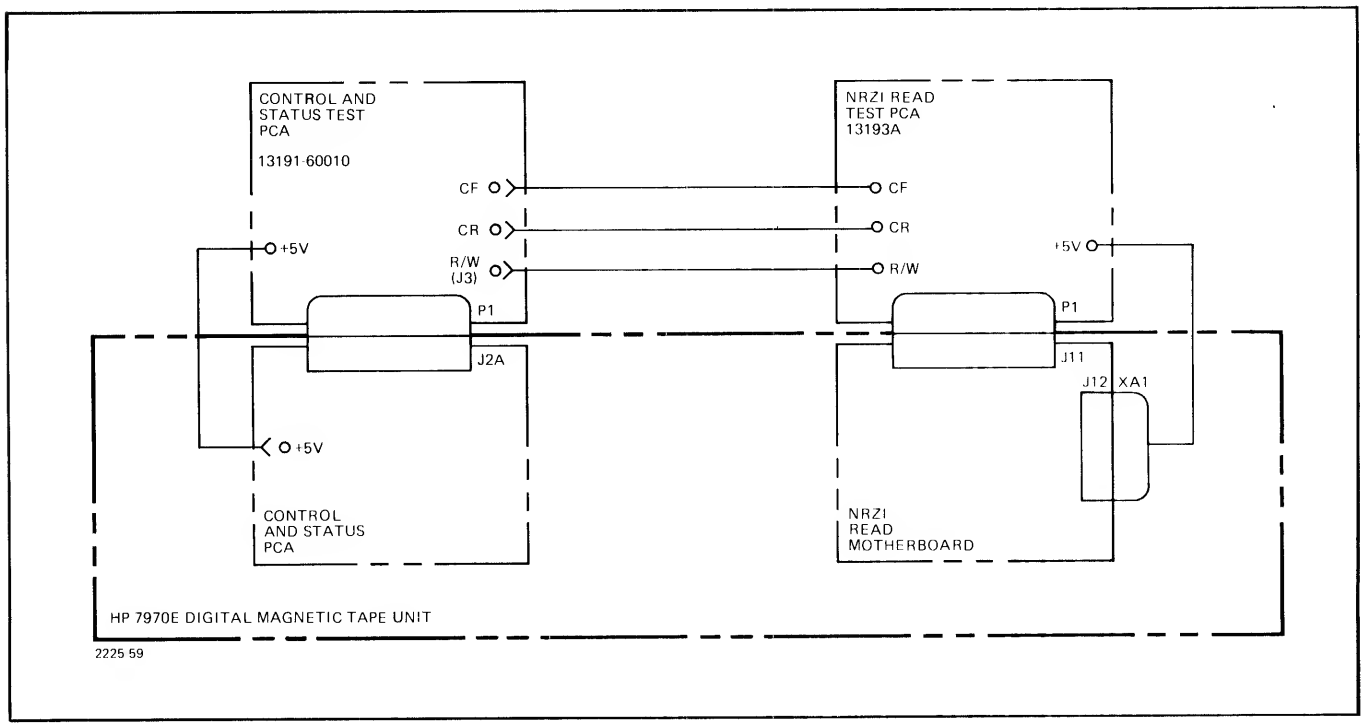


Figure 5-7. Test PCA Installation for Testing NRZI Circuits (7970 E Multiformat)

a. Read-Only Units. Preferred method where a read-after-write equipped tape unit is available.

1) On a separate unit with write capability, load the write test tape, place the tape unit in write mode, and write a full reel of all "1's" data at 200 cpi density. Do not rewind.

2) Transfer the test tape to the read only tape unit.

3) Read the tape in reverse.

4) Connect an oscilloscope to each preamplifier test point and adjust preamplifier gain variable resistors for an average Peak-to-peak output of 6.4 - 0.4, +0.2 Volts.

b. Read-Only Units. Method using a reference amplitude test tape.

1) Load the test tape (HP 5080-4547).

2) Operate the tape unit in read mode.

NOTE: Due to age and handling, a reference tape does not have the degree of magnetism that was originally written, thus gains set up to this standard will be set high. If this is suspected, the gains can be checked with recently written data tapes; the gain should range from greater than 4.0 VPP to less than 6.6 VPP.

3) Adjust preamplifier gain variable resistors to obtain the average peak-to-peak output voltage specified on the test tape reel tolerance specifications, $\pm$ 0.2 volts peak-to-peak.

c. Read/Write Units.

1) Load the transport with the write test tape and place the tape unit in write mode. Write all "1's" @ 200 cpi.

2) Connect an oscilloscope to each preamplifier test point and adjust each preamplifier for an output of 6.4 - 0.4, + 0.2 volts peak-to-peak.

5-33. ALTERNATE METHOD FOR PREAMPLIFIER GAIN ADJUSTMENT. Use only if means for writing 200 CPI are not available.

a. Write all ones on blank tape at a density of 800 CPI using the 13192A or appropriate controller.

b. Scope the test points on the Read Preamplifier PCA. Adjust associated gain potentiometer for 5.0V - 0.5, + 0.2V Peak-to-peak.

5-34. FORWARD STATIC SKEW COMPENSATION ADJUSTMENTS. The techniques for rapid adjustment and for evaluating the need for adjustment differ. Figure 5-8 shows poor skew alignment and proper skew alignment. To adjust static skew compensation proceed as follows:

a. Load the Master Alignment Tape, HP part number 9162-0027, and place the tape unit in synchronous forward mode for the adjustment operation.

b. Adjust FWD skew delay control of channel 2 (Read data PCA) until resistor is approximately ¼ turn from the fully CCW position. Channel 2 will be reference channel for the remaining adjustments.

c. Connect the oscilloscope channel A probe to the SKEW test point of the reference channel (2). Connect the oscilloscope channel B probe to each SKEW test point in succession and algebraically add oscilloscope channels A and B.

d. Adjust the oscilloscope sweep to display at least one full bit time (leading edge of one bit to the leading edge of the next), with the oscilloscope vertical deflection at approximately 2V/cm.

e. Adjust each channel skew delay variable resistor for a maximum displayed amplitude and test waveform as shown in figure 5-8.

5-35. REVERSE STATIC SKEW COMPENSATION ADJUSTMENTS. Reverse static skew compensation is accomplished in exactly the same manner as that used for forward skew except for the use of reverse drive mode and adjustment of reverse skew controls. The same SKEW test points are used for both adjustments.

5-36. READ CHARACTER GATE ADJUSTMENTS. The read character gate is adjusted to allow a period equal to approximately 46 percent of the bit-to-bit distance for all of the read bits in a character to be placed in the output register.

a. Load the tape unit with the Master Alignment Tape, HP part number 9161-0027 (or any all "ones" 800 cpi tape), place the unit in synchronous forward operation, and select 800 cpi operation (multiple density units only).

b. Synchronize the oscilloscope (negative slope) to the NOR test point on the read control card. (The first data bit of a character will start the gate time when this line goes to ground).

c. Observe the bit-to-bit time (negative-going edge to negative-going edge). The low (or ground) portion of this signal represents the character gate time.

d. Using the gate control (R29) on the read control PCA, adjust the NOR (ground portion) of the signal to 46 percent of the nominal bit-to-bit time. Ensure that the bit-to-bit time is consistent with the data transfer rate (i.e. 50 micro-seconds for a 7970 operating at 25 IPS - 800CPI).

NOTE: Figure 5-9 can be used as a guide once the reader is familiar with the forgoing procedures.

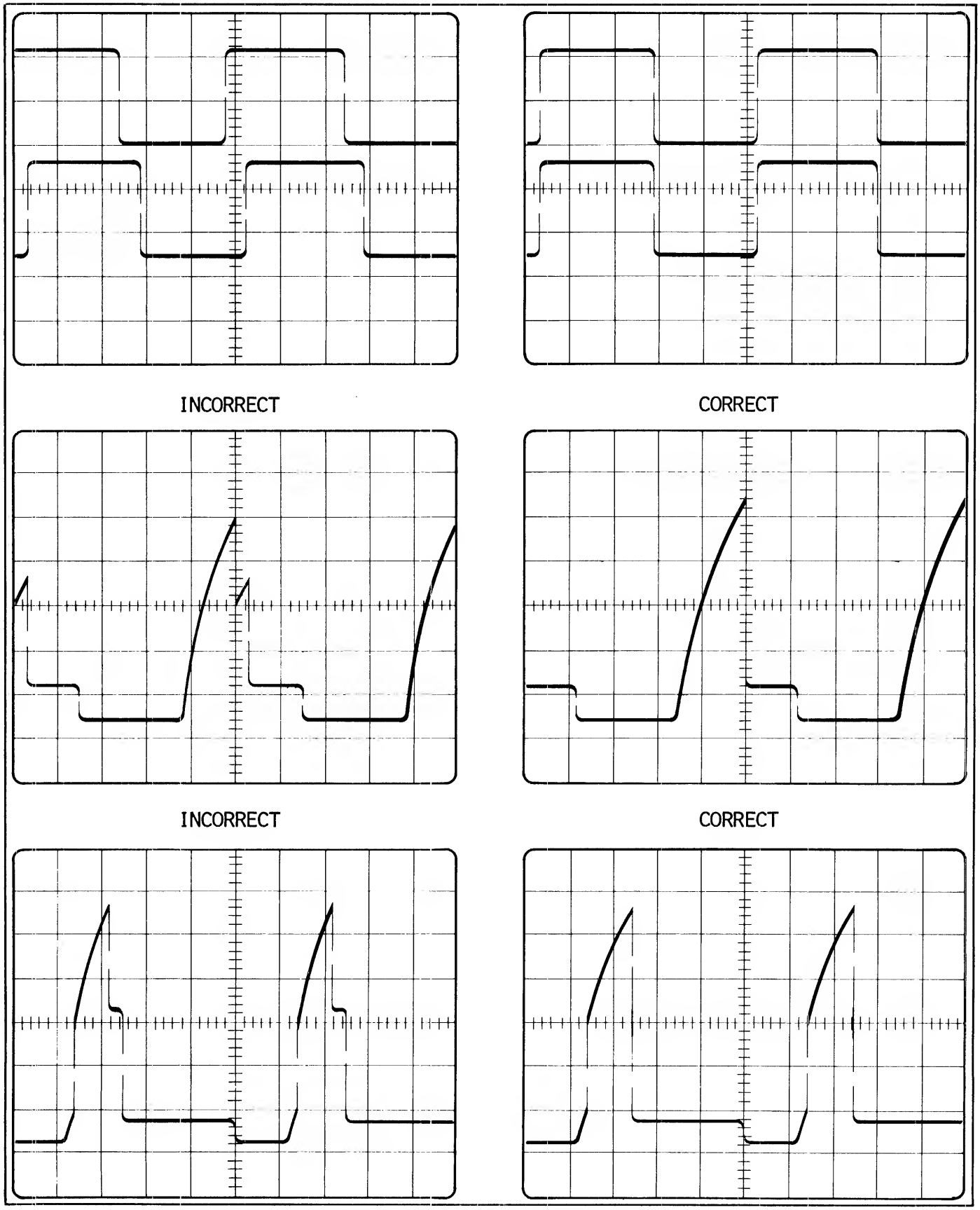


Figure 5-8. Skew Waveforms

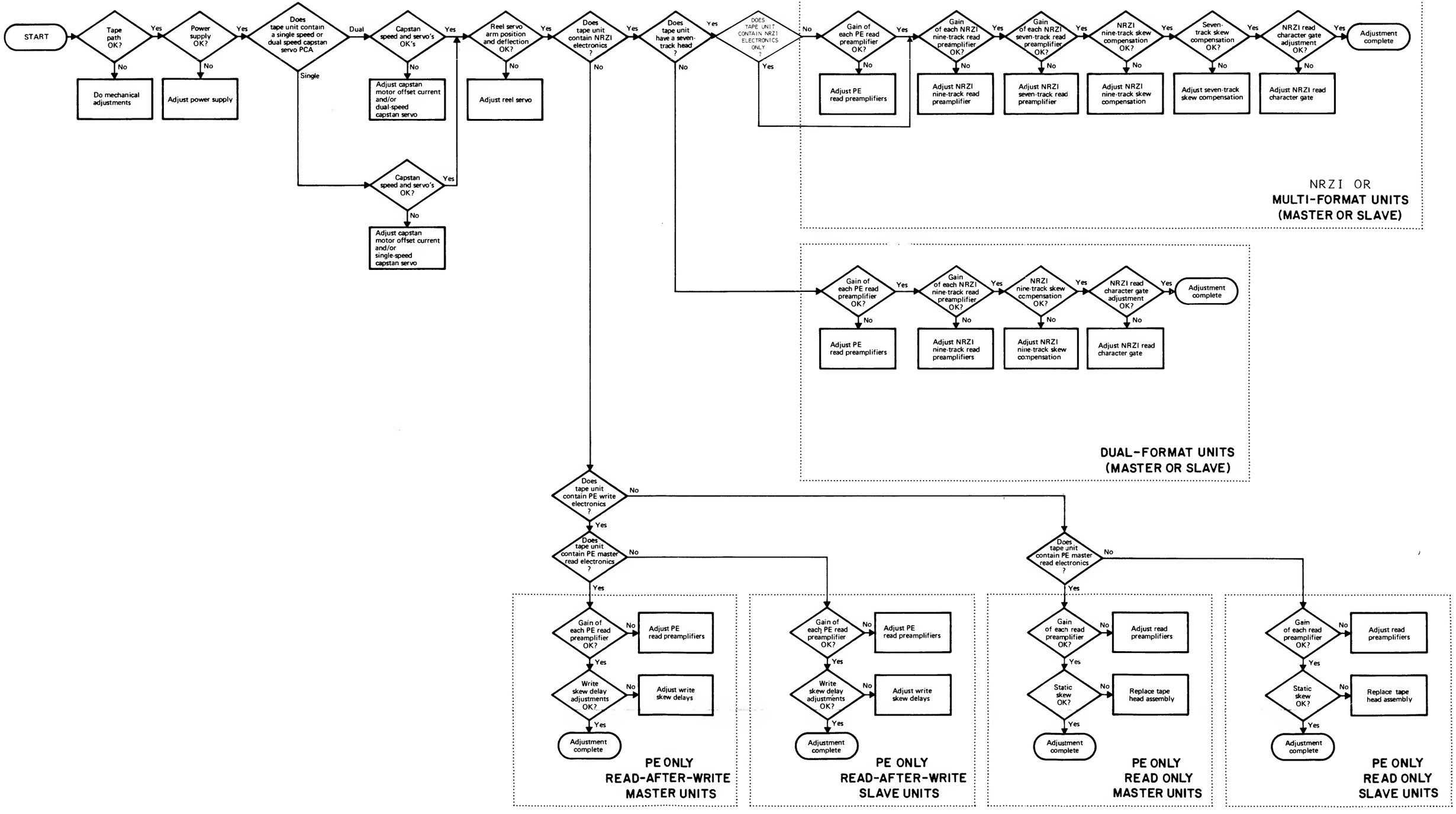


Figure 5-9. Adjustment Sequence Flowchart

5-41. TEST EQUIPMENT REQUIRED. Test equipment required to do performance tests on the PE read circuits is listed below.

a. Control and status test PCA, part number 13191-60010.

b. Read data test PCA, part number 13196-60000.

c. Oscilloscope, HP 180A dual trace, or equivalent.

d. Phase-encoded read circuits test tape, part number 5080-4555.

e. Write formatter PCA, part number 13195-60000. (May be part of normal tape unit configuration, if not, it must be installed for test purposes).

f. Write formatter test PCA part number 13196-60001.

g. Scratch certified 3200 frpi tape.

h. Reference amplitude test tape, part number 5080-4548.

i. Master alignment tape, part number 9162-0027.

5-42. TEST TAPE. The PE read data test tape (HP part number 5080-4555) is a 1200-foot pre recorded tape which can be used for performance testing and troubleshooting of the PE read circuits. It is divided into four sections by BOT and EOT reflective tabs.

5-43. Section 1 is a 450-foot section of nine-byte single-rotating bit pattern blocks. That is, each byte contains eight "0" data bits and one "1" data bit. The "1" data bit occurs once in each channel per block. The primary purpose of this section is to verify data recovery, data transfer, and data block detection.

5-44. Section 2 is a 100-foot section containing a 40-foot length of ID burst blocks, a 15-foot blank space and a length of file mark blocks. This section can be used to verify ID bursts and file marks.

5-45. Section 3 contains four 40-foot groups of PE data blocks in which the data of one channel is skewed a known amount. The data groups are separated by 15-foot inter-record gaps. Each block begins with a normal 41-byte preamble and is terminated with an 80-byte postamble. Due to methods of recording this section of tape, errors will sometimes occur between groups A, B, C, and D. This section verifies skew buffer operation. The long postamble allows verifications of postamble detection capability.

5-46. Section 3, group A is 40-feet of five-character blocks. The data pattern in channel P is 11111. The data pattern in channels zero through seven is 01010. Channel one is delayed by 1.5 byte times.

5-47. Section 3, group B is the same as group A except that channel one is delayed 2.5 byte times.

5-48. Section 3, group C is 40-feet of five-character blocks. The data pattern in channel zero is 11111. The data pattern in channels P and one through seven is 01010. Channel one is delayed by 1.5 byte times.

5-49. Section 3, group D is the same as group C except that channel one is delayed 2.5 byte times.

5-50. Section 4 is a 400-foot section containing blocks of ANSI format B data recorded while the tape speed is externally modulated to provide a short-term average density variation of ±15 percent. Section 4 is used to check the PE read system clocks ability to synchronize to incoming data.

5-51. PE READ CIRCUITS OVERALL PERFORMANCE TEST.

This test checks the ability of the PE read circuits to generate each output signal when the proper conditions exist. It is, therefore, an overall performance test of the PE read circuits. To perform the test, proceed as follows:

NOTE: If, due to repair, a unit is being realigned and set up, preamplifier gain adjustments (paragraph 5-63 thru 5-64) may be completed before the following steps. Normally it is advisable to leave the preamplifier gain adjustments alone while troubleshooting unless it is obvious the preamplifier is at fault.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install the following PCA's in the tape unit under test:

1) Control and status test PCA, part number 13191-60010.

2) Read data test PCA, part number 13196-60000.

c. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

d. Use the CF switch on the control and status test PCA (13191-60010) to set the tape in forward motion and check (on the read data test PCA) that the RC, EOB, and SD16 indicators are on and the MTE, STE, IDB, and TM indicators are off.

e. Connect the oscilloscope channel A probe to the parity channel preamplifier DIFF test point and adjust the sweep rate so that the block occupies 8 cm. Connect the trace B probe to the EOB test point on the read display test PCA. A single pulse should be present within ±0.3 cm of the 10 cm line (approximately 22 to 24 byte times from the end of the data block).

f. Connect the channel A oscilloscope probe to the RC (Read Clock) test point on the read data test PCA. Adjust oscilloscope sweep as necessary to verify that nine RC pulses occur for each zero volts line crossing of the signal on trace B. The RC pulse should be a negative pulse ($\overline{RC}$) with a duration of 2.5 $\pm$ 0.5 microseconds.

g. Connect the channel A oscilloscope probe to the P data bit test point on the read data test PCA (part number 13196-60000). Adjust the oscilloscope so that the spacing between the $\overline{RC}$ pulses is 1 cm and the negative-going edge of the $\overline{RC}$ pulse is at the first oscilloscope graticule line. The waveform at the P test point should be a negative pulse one cm wide. It should begin at the same time as the $\overline{RC}$ pulse and be active (low) during the first cm on the graticule.

h. Connect the Channel A oscilloscope probe to the read data test PCA test points for data channels zero through seven in turn. The pulse present at test points 0 through 6 should be the same as for test point P except that the channel zero pulse appears on the second cm of the graticule, the channel one pulse appears on the third cm, etc. The channel seven pulse should go low and remain low until the EOB pulse occurs.

i. Set the tape in reverse motion and check that the RC and EOB indicators on the read data test PCA are on, and the MTE, STE, and EVEN indicators are off.

5-52. SKEW BUFFER OVERFLOW DETECTION. This test checks the ability of the error detection circuits to detect a skew buffer overflow.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Use the CF switch on the control and status test PCA to set the tape in forward motion and, temporarily, short the DRDY test point on the master PE read control PCA to ground. The STE and MTE indicators on the read data test PCA should light and the RC indicator should be off.

5-53. SINGLE-TRACK ERROR VERIFICATION (STE). This test checks the threshold detector, low amplitude detector, and error detection circuits on the decoder PCA for each channel, the TIE decoder logic, and the single-track error and multiple-track error circuits in the state control logic. These circuits should light the STE indicator when a single track error is simulated on any channel. Also, the MTE indicator is checked to see that it does not light erroneously under single-track error conditions.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Use the CF switch on the control and status test PCA to set the tape in forward motion and temporarily short the DIFF test point, on the preamplifier PCA for channel P, to ground. The STE indicator on the read data test PCA should light and the MTE indicator should remain off (although it may flicker while the ground connection is made).

e. Repeat step d for channels zero through seven.

5-54. MULTIPLE TRACK ERROR VERIFICATION (MTE). This test verifies that the threshold detector, low amplitude detector, and error detection circuits on the decoder PCA for each channel and the TIE decoder logic and the MTE circuit in the state control logic are capable of detecting a low amplitude condition of the input signal on two channels from the preamplifiers. Also, the ability of the TIE decoder logic and MTE circuit to discriminate between a single-track error and a multiple-track error is checked.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Short the DIFF test point on the P channel preamplifier to ground.

e. Use the CF switch on the control and status test PCA to set the tape into forward motion and temporarily short the DIFF test point on the zero channel preamplifier to ground. The MTE indicator on the read test PCA should be on only while both DIFF test points are grounded.

f. Repeat step e for channels one through seven, in turn. (Ground any two to ground at the same time).

5-55. EVEN SIGNAL AND READ ONLY STATES PERFORMANCE TEST. This test checks that the error correction circuits generate an active EVEN signal when the required

conditions exist. It also checks that the state control logic passes through all read-only states (00, 01, 03, 07, 17, 12, 02, 16, 13 and 11) while reading a data block. This is done by determining that the RC signal becomes active during the reading of each data block. Since the $\overline{RC}$ signal is initiated in state 02, $\overline{RC}$ signals occurring in two successive blocks indicate the state control logic has passed from state 00, through the data loop (states 17, 12, 02, and 16), through state 11 and back through state 02.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

   (1) Control and status test PCA, part number 13191-60010.

   (2) Read data test PCA part number 13196-60000.

d. Short the LSB test point for the P channel decoder PCA to ground and use the CF switch on the control and status test PCA to set the tape into forward motion. The EVEN and MTE indicators on the read data test PCA should light.

e. Connect one oscilloscope probe to the RC test point on the read data test PCA. Connect the other oscilloscope probe to the DIFF test point on the P channel preamplifier and verify that two RC pulses occur for each block.

f. Remove the short on the P channel LSB test point and short, to ground, the LSB test point on the decoder PCA for each of channels zero through seven, in turn. For each channel, the EVEN and MTE indicators should light but only one RC pulse should occur per block.

5-56. FALSE PREAMBLE DETECTION PERFORMANCE TEST. This test checks that the state control logic will detect an improper preamble while passing through states 00, 04, and 05 in read-after-write mode.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

   (1) Control and status test PCA, part number 13191-60010.

   (2) Read data test PCA, part number 13196-60000.

d. Short the DIFF test point on the P channel preamplifier PCA to ground and set the tape into forward motion. The STE indicator on the read data test PCA should light.

e. With the P channel DIFF test point shorted, short the LWRITE test point on the data and status PCA to ground. The STE and MTE indicators on the read data test PCA should be on and the RC indicator should be off.

5-57. ID BURST DETECTION PERFORMANCE TEST. This test checks that the state control logic passes through the proper states (00, 01, 03, 13, and 11) when supplied an identification burst in read-only mode.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 2.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Set the tape in forward motion. Observe that the IDB indicator on the read data test PCA is on. The EOB indicator should light at the end of each block, and the RC, STE, and MTE indicators should be off.

e. The end of the IDB portion of this test can be distinguished by the absence of EOB. The IDB indicator will remain on until a different type of block is read.

5-58. TAPE MARK DETECTION PERFORMANCE TEST (TM). This test checks that the state control logic passes through the proper states (00, 01, 03, 13, and 11) when supplied a tape mark in read-only mode (step d). It also checks that a tape mark will not be detected if a faulty tape mark is supplied (steps e and f).

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Set the tape at the beginning of the tape mark part of section 2 of the test tape and set the tape in forward motion. The TM and EOB indicators on the read test PCA should be on. The RC, MTE, and STE indicators should be off.

e. Short the DIFF test point on the channel two preamplifier to ground. Bring the tape to the beginning of the tape mark part of section 2 and set the tape in forward motion. The TM indicator on the read data test PCA should remain off and both the MTE and EOB indicators should be on.

f. Repeat step e, shorting the DIFF test point on the channel six preamplifier instead of the channel two preamplifier. Again, the TM indicator should remain off and both the MTE and EOB indicators should be on.

5-59. SKEW CORRECTION PERFORMANCE TEST. This test verifies the ability of the decoder PCA skew buffers to correct skew. Steps d, e, and h of this test supply the channel one skew buffer with a signal which lags the signals in the other channels by 1.5 byte times. The skew buffers of the other channels should store the data for the first two bytes until the first data bit for channel one is stored in the channel one skew buffer. Step d checks skew buffer operation while the tape is running forward. Step e performs the same check with the tape running in reverse, thus also checking that the zero crossing enable logic is inverting the input signal in reverse mode.

The sections of tape used in steps d through g have identical data patterns in every channel (five data bits with the pattern 01010) except the parity channel which has a 11111 pattern (five data bits also). Steps h and i use sections of the tape which has an identical pattern (five data bits with the pattern 01010) in every channel except the zero channel which has a 11111 pattern.

Steps f, g, and i perform the same tests as steps d, e, and h, respectively, except that the channel one signal lags the others by 2.5 byte times instead of 1.5 byte times.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA part number 13196-60000.

d. Bring the tape to the beginning of part A of section 3. Set the tape into forward motion, observe the indicators on the read data test PCA while reading a short section of the tape, then stop tape motion. The RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should stay off.

NOTE: The above indicators are valid only during tape motion. Due to the method of recording this section of the tape, STE or MTE may occur between groups A, B, C, and D.

e. Set the tape into reverse motion and read the same portion of tape as in step a. Again, the RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should remain off.

f. Bring the tape to the beginning of part B, section 3. Set the tape into forward motion, observe the indicators on the read data test PCA while reading a short section of the tape, then stop tape motion. The RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should stay off.

g. Set the tape into reverse motion and read the same portion of tape as in step f. Again, the RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should remain off.

h. Bring the tape to the beginning of part C, section 3. Set the tape into forward motion, observe the indicators on the read data test PCA while reading a short section of the tape, then stop tape motion. The RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should stay off.

i. Bring the tape to the beginning of part D, section 3. Set the tape into forward motion, observe the indicators on the read data test PCA while reading a short section of the tape, then stop tape motion. The RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should stay off.

5-60. FALSE POSTAMBLE DETECTION PERFORMANCE TEST. This test checks that a false postamble will be detected by the state control logic in state 15. Steps d through g perform this check for read-only mode. Steps h and i perform the check for read-after-write mode. In the read only mode check, the state control logic passes through states 00, 01, 03, 07, 17, 12, 02, 16, 15, 13, and 11. In the read-after-write mode check, the state control logic passes through states 00, 04, 05, 07, 17, 12, 02, 16, 15, 13, and 11.

The taped data produces a false $\overline{\text{EOD}}$ signal to set the state control logic into state 15 (the postamble verification state) on the second data byte. In state 15, the fact that the SBEZ signal is not active on the third byte (because the third byte contains data) will produce an active $\overline{\text{MTE}}$ signal.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit.

c. Install the following PCA's in the tape unit under test:

(1) Control and status PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Bring the tape to the beginning of part A, section 3. Use only part A for this test. Do not over run into part B.

e. Short the DIFF test point on the P channel preamplifier and set the tape into forward motion. The STE, MTE, EOB, and RC indicators on the read data test PCA should be on and the EVEN indicator should be off.

f. Remove the short from the P channel DIFF test point and short the DIFF test point on the channel zero preamplifier to ground.

g. Set the tape into forward motion. The RC, STE, and EOB indicators on the read data test PCA should light and both the EVEN and MTE indicators should remain off.

h. Bring the tape to the beginning of part A, section 3.

i. Short the LWRITE test point on the data and status PCA to ground and set the tape into forward motion. The MTE, and EOB indicators on the read data test PCA should light. The EVEN, RC, and STE indicators should remain off.

5-61. CLOCK SYNCHRONIZATION PERFORMANCE TEST. This test checks the clock and clock control logic synchronization function while reading a section of tape with a short-term density variation of ±15 percent. Step d checks the ability of the clock to keep synchronized to the incoming data. Steps e and f check that the clock control logic will synchronize the clock to the parity channel Sync Pulse when the channel two Sync Pulse is disabled. Step g checks that the clock control logic causes the clock to operate at its fixed frequency in read-after-write mode.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Bring the tape to the beginning of section 4. Set tape into forward motion and read the tape for at least 30 seconds. The RC and EOB indicators on the read data test PCA should light and the STE and MTE indicators should remain off.

e. Bring the tape to the beginning of section 4 and short the DIFF test point on the channel two preamplifier to ground.

f. Set the tape into forward motion and read the tape for at least 30 seconds. The STE indicator on the read data test PCA should light and the MTE indicator should remain off.

g. Remove the short from the channel two DIFF test point and short the LWRITE test point on the data and status PCA to ground. Set the tape into forward motion. The MTE indicator should alternate between an on and off condition. STE and EVEN may randomly blink on and off.

5-62. STATUS LOGIC PERFORMANCE TEST. This test checks the portion of the status logic which controls the $\overline{SD16}$ and the MREV signals. The other signals generated by the status logic are checked by other performance tests. Steps d through h check the logic which generates the $\overline{SD16}$ signal. Step i checks the MREV signal as initiated by the $\overline{REV\ 1}$ signal from a slave unit.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

c. Install a scratch tape in the tape unit.

d. With the tape unit selected and on line (a high present at TP3 on control and status PCA) and the tape stopped, check that the SD16 indicator on the read data test PCA is on.

e. Disconnect the unit select jumper on control and status test PCA (13191-60010). This de-selects the tape unit. Then reconnect the jumper; the SD16 indicator should be off while the jumper is disconnected.

f. If the tape unit has an 800 density switch, select 800 density; then select 1600 density. The SD16 indicator should be off while 800 density is selected.

g. Place the tape unit off line by pressing the RESET pushbutton on the tape unit front panel. The SD16 indicator should be off.

h. With the tape unit still off line, short pins 24 and 24X together at connector J16 on the master PE read motherboard. The SD16 indicator should be on while the two pins are shorted together.

i. Set the tape into forward motion and short pins 23 and 23X at slave connector J16 on the PE master motherboard. The MTE indicator on the read data test PCA should light while the short is in place.

5-63. PE READ PREAMPLIFIER GAIN PERFORMANCE TEST (READ-ONLY UNITS). Before performing the following procedures, ensure that the tape transport long-term speed variation is within specification. To check the preamplifier gain, proceed as follows:

a. Install reference amplitude test tape, part number 5080-4548, in tape unit.

b. If the tape unit under test has 1600 density select switch front panel, select 1600.

c. Connect oscilloscope probe to DIFF test point on read preamplifier PCA for parity channel (PE test point on seven/nine-track tape units).

d. Set tape into forward motion at synchronous speed using CF switch on control and status PCA. Observe waveform, average peak-to-peak amplitude should be 4.0 $\pm$ 0.1 volts.

NOTE: Due to age and handling, a reference tape does not have the degree of magnetism that was originally written, thus gains set up to this standard will be set high. If this is suspected, the gains can be checked with recently written data tapes; the gain should be set as close to 4.1 VPP as possible.

e. Repeat steps c and d for each of the remaining channels (zero through seven).

5-64. PE READ PREAMPLIFIER GAIN PERFORMANCE TEST (READ/WRITE UNITS). Before performing the following procedures, ensure that the tape transport long-term speed variation is within specification. To check the preamplifier gain of read/write units, proceed as follows:

a. Install a scratch certified 3200 frpi tape in tape unit.

b. Install control and status test PCA, part number 13191-60010, PE write formatter, part number 13195-60000, and write formatter test PCA, part number 13196-60001 in the tape unit.

c. Connect oscilloscope probe to DIFF test point of read preamplifier for the parity channel and set up the test PCA's listed in step b as follows:

Write formatter test PCA. Test plug in position corresponding to tape drive speed.

PE Write Formatter. Data Select-1600 frpi Data Block-ON.

Control and Status WSW-ON (up) CF-ON (up).

d. The tape unit is now writing continuous 1600 frpi in all nine channels. Measure average peak-to-peak amplitude of signal as shown in the oscilloscope at DIFF test point. The oscilloscope should read 4.5 $\pm$ 0.3 Vpp. Adjust gain potentiometer, if necessary, to this specifications.

NOTE: A feed-through signal (crosstalk) from the write head can cause minor distortion on the DIFF test point signal. The limits indicated in step d refer to portions of the test point signal which are free of obvious write head feed-through distortion.

Adjust oscilloscope to display several cycles of DIFF test point signal. Waveforms should be free of clipping and discontinuities (ignore slight distortion caused by crosstalk).

f. Repeat steps c through e for each of the eight remaining channels.

5-65. PE THRESHOLD LEVEL PERFORMANCE TEST (READ-ONLY UNITS). To check the threshold level of a PE master read-only tape unit, proceed as follows:

a. Install a scratch tape in the tape unit.

b. Connect the common (ground) lead of a dc voltmeter, with an accuracy of one percent or better, to the GND test point on the PE data and status PCA (master units) or the GND test point on the PE slave read PCA (slave units).

c. Set tape unit into forward tape motion and use voltmeter to check voltage at +THR and -THR test points on PE data and status PCA. They should be as follows:

+THR: +0.30 ± 0.02 Vdc.
-THR: -0.30 ± 0.02 Vdc.*

* -THR used on 07970-62041 PCA only

5-66. PE THRESHOLD LEVEL PERFORMANCE TEST (READ/WRITE UNITS). To check the threshold level of a PE read/write tape unit, proceed as follows:

a. Install a scratch tape in the tape unit.

b. Connect the common (ground) lead of a dc voltmeter, with an accuracy of one percent or better, to the GND test point on the PE data and status PCA (master units) or the GND test point on the PE slave read PCA (slave units).

c. Connect a source of +5 Vdc to TP1 (WSW signal) of the control and status PCA.

d. Set tape unit into forward tape motion and use voltmeter to check voltage at +THR and -THR test points on PE data and status PCA. They should be as follows:

+THR: +0.77 ± 0.02 Vdc.
-THR: -0.77 ± 0.02 Vdc.*

* -THR used on 07970-62041 PCA only

5-67. STATIC SKEW PERFORMANCE TEST. Before performing the following test, ensure that the tape transport is operating properly. To check the static skew, proceed as follows:

a. Install master alignment tape, part number 9162-0027, in tape unit.

NOTE: Waveforms for a slave unit can be monitored at the DAT test points on the read decoder PCA's in the master unit, provided the slave unit is connected to the master unit and selected on the master unit select switch. If the slave unit is not connected to the master unit, monitor the waveforms at the test points on connector P2 of the slave read PCA. The test point for master units is the DAT test point on the read decoder PCA.

b. Connect oscilloscope channel A probe to test point for parity channel.

c. Connect oscilloscope channel B probe to DAT test point on read decoder PCA for channel two. (Channel two is used as the reference channel).

d. Set tape unit for synchronous speed forward and adjust oscilloscope sweep to trigger on positive edge of whichever waveform goes positive first. (If parity channel waveform goes positive before channel two waveform, trigger oscilloscope sweep on parity channel waveform; otherwise trigger oscilloscope sweep on channel two waveform).

e. Adjust oscilloscope for alternate display of channels A and B.

f. Estimate and record average time difference between positive edges of waveforms. Also, record whether parity channel waveform occurs before or after channel two waveform.

g. Repeat steps b and d through f for channels zero, one, and three through seven. Leave oscilloscope trace B connected to channel two (reference channel).

h. Add largest time difference by which a waveform precedes channel two waveform plus largest time difference by which a waveform follows channel two waveform.

i. Multiply sum of largest leading and lagging time differences (in microseconds) by tape speed (in inches/second) to obtain static skew in microinches. Skew should be less than 300 microinches.

5-68. CHECKOUT PROCEDURES.

Checkout procedures for the tape unit consist of visual checks and checks for proper tape movement. Included are power-off checks, control checks, and a tape path check.

5-69. POWER-OFF CHECKS.

Preliminary power-off checks are performed as follows:

a. Tape Rollers: The tape rollers must operate freely and have no excessive end play.

b. Head Crosstalk Shield (installed on read/write units only): The head crosstalk shield should operate freely and should have clearance between face of head and shield (room to slip a punched card through without binding).

c. Reel Servo Arm Limit Switches: The three limit switches associated with the reel servo arms must operate when the arm is approximately 1/8 inch from the rubber stop. The roller on the switch arm should be approximately on the center of the arm when the arm is fully against the stop. There should be positive travel of the switch lever beyond the point at which it actuates the micro-switch. The check can be made audibly if ambient noise level permits, or with an ohmmeter if room noise is too high.

d. Write Enable Sensing: The write enable sensing finger nominal location dimensions should be as follows:

   (1) The distance between the outside surface of the write enable sensing finger and the outside flange diameter of the reel turntable should be 3/32-inch (nominal).

   (2) In the file protected position (inoperative), the dimension between the outer tip of the sensing finger and the outer face of the reel turntable should be 3/16-inch (nominal) above the turntable surface.

(3) In the write enable position (with solenoid energized) the outer tip of the sensing finger should be 1/16-inch below the turntable surface.

(4) The sensing finger must not touch the turntable under any condition.

e. Reel Retaining Knob: With the locking lever released, the reel should slip over the rubber grip ring easily, and it should be possible to easily rotate the reel. When the lever is closed, positive resistance should be felt as the rubber is compressed. In the locked position, it should not be possible to move the reel by hand. If slippage is suspected, place a piece of masking tape on the reel, and another on the hub. A mark placed in alignment on both pieces of tape should not become misaligned by more then 1/8 inch in 16 hours of operation. To correct tape reel slippage, release locking lever and loosen the pozidrive screw, rotate the reel retainer knob clockwise, and tighten the screw. Repeat until tape reel mounts firmly and does not slip.

5-70. CONTROL CHECKS.

Verify position of 115/230 volt selector switch; connect unit to appropriate power source and check the following operating modes.

5-71. TAPE LOADING AND WRITE ENABLE. Place a reel of tape (with write enable ring) on unit and thread with the power switch on and the safety switch in normal position (achieved by first closing and then opening the cover door). After threading tape, press LOAD and verify that the following takes place.

a. Tape tension is established. RESET indicator comes on.

b. WRITE ENABLE indicator comes on (if unit contains a write enable assembly).

c. All controls are inoperative, no sequence of commands can initiate tape movement.

5-72. ON-LINE TRANSFER AND RESET. If the tape unit contains the unit select option, place the control and status PCA unit select jumper to the OFF pin (this is not the same as OFF on unit select option). Otherwise, set the unit select jumper on the control and status PCA to the correct unit select position. Then load the tape. Following completion of a load sequence with tape positioned at loadpoint, (LOAD indicator on) press ON LINE and verify that unit will respond to external controller commands. Pressing ON LINE while loadpoint search is in process during the LOAD sequence will also result in ON LINE operation upon completing the search (LOAD indicator is ON). While ON LINE: the unit will not respond to local controls with the exception of RESET.

5-73. DYNAMIC BRAKING AND RECOVERY FROM POWER FAILURE. Place unit in rewind mode after tape is well into take-up reel. When full rewind speed is reached, turn power switch off to simulate power failure. Tape should stop without any da-

to tape and without throwing a tape loop. Proceed with recovery to on-line status by following normal load sequence. Except that when tape unit goes into the load-point search mode, loadpoint tab must be simulated by pressing the RESET button. This can then be followed by an on-line command.

5-74. REWIND OPERATION. The front panel REWIND control is effective only while the unit is in the reset state which permits local control. The rewind command will override the load command and will return the tape to the loadpoint position (LOAD indicator on with tape stopped). Rewind may be terminated prior to loadpoint by pressing RESET. Transfer to on-line is also possible immediately following this sequence.

5-75. TAPE PATH MECHANICAL CHECK.

With undamaged tape threaded on the tape unit and with the unit in the appropriate operating mode, evaluate the following characteristics of the tape path.

a. Capstan Height: Capstan height should be such that the tape is guided equal distance in from the outer and inner edge of the capstan. The air escape grooves provide a means for judging.

b. Tape Tracking Over the Tape Rollers: Tracking over the guides should be smooth with no evidence of edge forces anywhere in the tape path. Transverse reflected light may be used to assist in judging. Light reflections across the 1/2-inch width of the tape should not be bent due to points of stress.

c. Photosense Position: Face of photosense head assembly should be parallel to the path of the tape and positioned approximately 1/8 inch from the tape.

5-76. PERFORMANCE TESTS.

The performance tests on the tape unit verify operation within specifications. Included are performance tests on the power supply, transport circuits, control circuits, PE read circuits, PE write circuits, and the NRZI circuits.

NOTE: To perform an overall performance test on the tape unit circuits, perform the power supply performance tests (paragraph 5-77), the control checks (paragraph 5-70). The PE read circuits performance test (paragraph 5-96), the PE write circuits overall performance test (paragraph 5-124), and the NRZI circuits overall performance test (paragraph 5-132).

5-77. POWER SUPPLY PERFORMANCE TESTS.

Performance testing of the power supply consists of voltage checks on the regulated and unregulated supply voltages.

5-78. TEST EQUIPMENT REQUIRED. Test equipment required for power supply testing consists of the following:

a. Multimeter/counter HP 5306A or equivalent.

b. Oscilloscope, HP 180 Dual Trace or equivalent.

5-79. REGULATED SUPPLY VOLTAGES Regulated voltages shall remain within tolerances over a primary voltage range of ± 10 percent. DC voltages and tolerances are to be as specified below. The peak-to-peak ripple values are nominal and minor variances may be expected. Ripple is stated under tension-only conditions.

a. The +5 volt supply must be +5.000 ±0.050 Vdc.

b. The ±12 volt supplies must be 12.000 ±0.360 Vdc.

5-80. UNREGULATED SUPPLY VOLTAGES. Unregulated supply voltages are a direct function of line voltage. The following table of nominal values should be judged only at a line voltage of 115 volts. RMS ripple values are nominal and apply at 60 Hz.

a. ±40 Vdc: Nominal value is ±57 volts; ripple of 150 mv p-p (sawtooth).

b. +20 Vdc: Nominal value is 23 volts; ripple of 600 mv p-p (sawtooth).

c. -20 Vdc: Nominal value is -23 volts; ripple of 300 mv p-p (sawtooth).

d. +10 Vdc: Nominal value is +12 volts; ripple of 900 mv p-p (sawtooth).

5-81. TRANSPORT PERFORMANCE TESTS.

The transport performance tests consist of measuring capstan motor offset current, measuring tension arm position and deflection, measuring long term speed variation (tape units capable of reading data), measuring start and stop time and distance, measuring instantaneous speed variations, and measuring fast forward, reverse, start, and stop times. Included is a dynamic tape skew check for tape units equipped with read and write electronic circuits.

NOTE: The following procedures (paragraphs 5-82 through 5-95) apply to tape units with either single-speed or dual-speed capstan servo printed-circuit assemblies.

There are three service switches incorporated in the capstan servo PCA. These together with the REWIND and LOAD controls provide a means of operating all five drive modes for service and/or adjustment purposes. There is no capability for cyclic drive operation incorporated in the tape unit.

The HP 13191A Control and Status Test Board Accessory is available for use with the tape unit. With this test board it is possible to completely adjust and verify the performance of the control and status function of a tape unit under off-line conditions. Complete details covering this item is included with the accessory. The HP 13191A Control and Status Test Board Accessory provides a normal drive modes as well as cyclic programming which is suitable for adjustment of the capstan start-stop ramp. The test board also includes status indicator lamps to verify all normal status functions. The test board is installed in the connector of the tape unit control and status PCA.

5-82. TEST EQUIPMENT REQUIRED. Test equipment required for performance testing of the tape transport is as follows:

a. Control and status test PCA, part number 13191-60010.

b. Oscilloscope, HP 180, dual trace or equivalent.

c. Multimeter/counter 5000A or equivalent.

d. Master alignment tape, part number 9162-0027.

e. Transport speed test tape, part number 5081-9401.

5-83. CAPSTAN MOTOR OFFSET CURRENT. Connect a suitabe dc voltmeter or oscilloscope across the 1.5 ohm, 1 percent resistance (comprised of R21 and R22 in parallel). The common sides of the resistors are connected to pin 2 of CJ-1. With the tape under tension but not tape motion, the voltage should not exceed the following (reference to 0 Vdc).

a. Maximum acceptable operating limit: $\pm$100 mV dc at 25°C.

b. Adjustment recommended if greater than: $\pm$80 mV dc. (Refer to alignment section).

5-84. LONG-TERM SPEED VARIATION. The long-term tape speed variation is measured by using a frequency counter to count the signals at the output of one of the read preamplifiers while reading a tape with highly accurate between-character spacing. The signal frequency at the preamplifier output is used as a measure of tape travel per second, HP transport speed test tape, part number 5081-9401, provides a between-character spacing accuracy better than 0.1 percent. Reference frequencies listed below are based on use of this tape. To check long-term speed variation, proceed as follows:

a. Connect a frequency counter to the output of the channel three preamplifier.

b. Install transport speed test tape, part number 5081-9401.

c. Use the three switches on the capstan servo printed-circuit assembly and the REWIND switch on the front panel to control tape motion while checking the tape

speeds listed below.

NOTE: To derive tape speed frequencies not supplied, use the following equation:

FREQUENCY (in Hz) = 333.33 X TAPE SPEED (in ips)

(1) Forward and Reverse Drive: Frequency depends on tape speed and must be calculated for speeds other than 25 ips, 37.5 ips and 45 ips which are listed below. Maximum acceptable operating limit is based on ±1 percent with adjustment recommended if speed error is +0.8 percent or greater.

a. The 25 ips drive nominal frequency is 8,333 Hz. Acceptable limits are ±83 Hz.

b. The 37.5 ips drive nominal frequency is 12,500 Hz. Acceptable limits are ±125 Hz.

c. The 45 ips drive nominal frequency is 15,000 Hz. Acceptable limits are ± 150 Hz.

(2) Loadpoint Search: 20 ips; basic frequency is 6,667 Hz.

a. Maximum acceptable limit is ±1,330 Hz (±20 percent).

b. No adjustment is provided.

NOTE: The half-speed forward and half-speed reverse checks, as listed below, are applicable only to tape units with a dual-speed capstan servo printed-circuit assembly.

(3) Half-Speed Forward and Half-Speed Reverse: 22.5 ips, basic frequency is 7,500 Hz.

a. Maximum acceptable limits are ±75 Hz (±1 percent).

b. Adjustment recommended if greater than ±60 Hz (±0.8 percent).

(4) High-Speed Forward: 160 ips, basic frequency is 53,333 Hz.

a. Maximum acceptable operating limit: ±1,050 Hz (±2 percent).

b. Adjustment recommended if greater than: ±800 Hz (±1.5 percent).

(5) Rewind (High-Speed Reverse): Checked identically to the limits applicable to high-speed forward, except that the rewind mode is used.

5-85. TENSION ARM POSITION. With no tape motion, the tension arms should be aligned with the centering marks on the rear of the casting. Adjustment is required if the arm is out of position by more than the diameter of the arm.

5-86. TENSION ARM DEFLECTION. The amount of tension arm deflection during tape motion is dependent on the tape speed and the amount of tape on the associated reel. At the highest speed (45 ips), providing there is less than 100 feet of tape on the reel associated with the tension arm (the upper reel is associated with the upper tension arm and the lower reel is associated with the lower tension arm), the tension arms should deflect to the outer marks on the back side of the main casting (in both forward and reverse modes). At lower speeds the deflection should be proportionately less. For example, at 22-1/2 ips, under the same conditions, the deflection should be approximately half the deflection at 45 ips.

5-87. START TIME MEASUREMENT. Start measurement (for both forward and reverse motion) consists of measurement of the start ramp delay time and the start ramp 90 percent time for both forward and reverse tape motion. To make these measurements, it is necessary to apply rapidly alternating active and inactive conditions (squarewave signal) of the $\overline{\text{FWD}}$ (or $\overline{\text{REV}}$) signal to the capstan servo printed-circuit assembly (PCA). This produces repetitious start ramps for oscilloscope display. (The $\overline{\text{FWD}}$ signal is accessible at TP9 of the control and status PCA. The $\overline{\text{REV}}$ signal is accessible at TP 5 of the PCA). Time duration of the active and inactive levels of the $\overline{\text{FWD}}$ (or $\overline{\text{REV}}$) signal must be greater than the 100 percent time of the start ramp to be measured. (The start ramp time is variable, depending on tape speed).

NOTE: On dual speed tape units, check both the start and stop ramp delay time.

5-88. Start ramp delay time. To measure the start ramp delay time, proceed as follows:

a. Connect the oscilloscope probe to the FWD/REV test point on the capstan servo PCA.

b. Synchronize the oscilloscope sweep on the negative edge of the $\overline{\text{FWD}}$ signal at TP9 on the control and status PCA (for measurement of the start ramp delay time in forward tape motion) or at TP5 ($\overline{\text{REV}}$ signal) of the control and status PCA (for reverse tape motion).

c. Measure the start ramp delay time for both forward tape motion and reverse tape motion. The start ramp delay time is the time interval between the start of the oscilloscope sweep and the time the ramp waveform reaches 3 percent of its steady-state value. The start ramp delay time, for both forward and reverse tape motion, should be 0.5 ± 0.5 ms.

5-89. Start ramp 90 percent time. To measure the start ramp 90 percent time, proceed as follows:

a. Connect the oscilloscope probe to the FWD/REV test point on the capstan servo PCA.

b. Synchronize the oscilloscope sweep on the negative edge of the FWD signal at TP9 on the control and status PCA.

c. Start tape motion and measure the start ramp 90 percent time, for both synchronous speed forward and synchronous speed reverse tape motion. The start ramp 90 percent time is the time interval on the start ramp, from 0 volts to 90 percent of the steady-state value. This time is dependent on tape speed. Values for some common tape speeds are listed below. For any unlisted speeds, use the following equation to derive start ramp 90 percent time:

$$T = \left(\frac{.375}{\text{Speed (ips)}} - .001\right) (.9)$$

Table 5-2. Capstan Servo Start/Stop Time

SPEED (ips)	TIME (90%)
12.5	26.1 ms ± .5 ms
18.75	17.1 ms ± .2 ms
22.5	14.1 ms ± .2 ms
25.0	12.6 ms ± .2 ms
37.5	8.1 ms ± .1 ms
45.0	6.6 ms ± .1 ms

5-90. INSTANTANEOUS SPEED VARIATION. The instantaneous speed variation check is made using a standard test tape on which a constant frequency is written. The oscilloscope is connected to the output of the read preamplifier and one period of the signal present at that point is displayed. The horizontal jitter of the zero crossover point, along the zero-volt line, is then used as a measure of the instantaneous speed variation. To measure the instantaneous speed variation, proceed as follows:

a. Install transport speed test tape, part number 5080-4525, in the tape unit.

b. Connect the oscilloscope probe to the test point at the output of the read preamplifier for channel three.

c. If the tape unit contains a density select option, select density 1600.

d. Adjust the oscilloscope so that one full period of the signal is exactly 10 centimeters in width.

e. Select X10 magnification of the oscilloscope sweep.

f. Measure the amount of peak-to-peak horizontal jitter along the zero-volt line. It should not exceed 6 centimeters (6 percent peak-to-peak jitter).

5-91. DYNAMIC TAPE SKEW. Dynamic tape skew is that variation in tape velocity which generates a differential time position between the two outermost tracks on the tape. Measurement is made as follows:

a. Install master alignment tape, part number 9162-0027, in tape unit.

b. Use dual trace oscilloscope and connect to preamplifier output of the two outside tracks (channels four and five). Use chopped mode (triggered by channel A) with the main sweep synchronized for a positive slope trigger at the zero axis crossover. (Use negative slope in reverse direction).

c. Adjust both channel gains and positions to superimpose the two waveforms (amplitude only; there will be varying degrees of time difference due to static skew characteristics).

d. Use the delayed sweep feature to present the next (one bit-to-bit distance later) zero axis crossover on the delayed sweep. The delayed sweep must be on internal sync, triggered on the negative slope. (Use positive slope in reverse direction). The earliest of the two tracks will sync the delayed sweep and the other will arrive later and will have jitter that represents the time differential in microseconds peak-to-peak. Again gains must be adjusted as high as possible (both the same) and the delayed sweep trigger set for maximum stability of the stable waveform. There will be a considerable dead zone in the delaying sweep adjustment. Use the first operating position as the sweep is moved out from minimum delay position. There is no significance to the time differential between the stable and unstable waveforms. Also this does not represent static skew as the difference is a function of oscilloscope gain and position settings.

e. Measure the peak-to-peak time band of the unstable waveform as it crosses the zero axis. Convert this to microinches peak-to-peak for the tape speed involved. Worst case must not exceed $\pm$50 microinches (100 microinches peak-to-peak) and applies to forward or reverse mode.

5-92. FAST FORWARD/REVERSE START/STOP CHARACTERISTICS. Fast forward and fast reverse characteristics are measured by synchronizing an oscilloscope with the appropriate drive command, and observing the dc output of the tachometer using the TACH test point on the capstan servo card.

CAUTION

Do not issue sequential fast drive commands without allowing time to read full speed or to return to zero speed. Failure to observe this precaution may cause excessive power dissipation in the reel servo amplifier circuitry. Minimum time between commands should be one second or the sum of the start and stop times (whichever is greater).

Fast forward/reverse start or stop times are measured by observing the time (following a start or stop command) required for the tachometer output to either reach its maximum value (for start time) or to fall to zero (for stop time). Nominal times are from 400 to 700 milliseconds. Typically, the value will be 600 milliseconds.

Fast forward/reverse start or stop distances are determined by the time required for the ramp to move from one state to the other. This time is nominally 500 milliseconds. One-half of this time multiplied by 160 ips equals the nominal start/stop distance of 40 inches.

5-93. FUNCTION COMMANDS. Select CS: The control and status PC assembly includes a unit select jumper that can serve to establish unit identification where the front panel unit select option is not present. If no select function is desired, the jumper can be placed in the OFF position which will permit response to controller commands, when the unit is on-line with load sequence completed, and is not rewinding. Verify the following conditions to check the select (CS) line:

a. Unit responds to commands with jumper connected to OFF.

b. Unit responds to 0 through 3 positions when corresponding CS0 through CS3 is selected by the controlling device.

c. When front panel select option is included, place internal jumper in the off position and verify that response to pushbuttons 0 through 3 is same as in step b above. When the front panel OFF pushbutton is pressed, unit must not respond to any commands from the controlling device.

Verify that the off-line (CL) line clears the write condition and returns the selected tape unit to the reset condition.

5-94. MOTION COMMANDS. Verify that the following external commands will place the selected and on-line tape unit in the corresponding drive mode:

a. Forward (CF): Tape drives forward.

b. Reverse (CR): Tape drives reverse and stops at loadpoint tab.

c. Rewind (CRW): Tape unit enters rewind mode, remains on-line.

d. High Speed (CH): Tape unit will respond only when this is combined with either a forward or reverse command. When so combined, tape will drive at 160 ips speed. CH with CR will drive reverse past loadpoint.

CAUTION

Do not issue sequential fast drive commands without allowing time to reach full speed or to return to zero speed. Failure to observe this precaution may cause excessive power dissipation in the reel servo

amplifier circuitry. Minimum time between commands should be 1 second or the sum of the start and stop times (whichever is greater).

5-95. STATUS OUTPUTS. Verify that the following status outputs are high when a selected and ready tape unit is in the condition indicated.

a. On-Line (SL): High when selected tape unit has been manually placed on-line.

b. Ready (SR): High when selected unit is on-line, tape loading cycle is completed, and tape unit is not in rewind mode.

c. Load Point (SLP): High when selected tape unit has tape positioned at loadpoint reflective strip.

d. Density (SD2, SD5, SD8, and SD16): Verify that selected tape unit will display the density selected by the tape unit density switch if this option is present. Without this option, the tape unit will be set at 800 cpi but there will be no SD8 output.

e. Rewind (SRW): Verify that this status remains high as long as the selected unit is in the rewind mode. SRW must remain high until tape is repositioned at loadpoint tab.

f. File Protect (SFP): High when selected unit is not write-enabled.

g. End-of-Tape (EOT): High when selected unit has moved end-of-tape tab beyond photosense head. Will remain high until tab again passes photosense head in the reverse direction.

h. Phase Encode Status (SPE): Low when tape unit is ready to operate at density rate of 1600 CPI.

5-96. PHASE ENCODED READ CIRCUITS PERFORMANCE TESTS.

The PE read circuits performance tests consist of an overall performance test, which checks all PE read circuit outputs, and other tests which check selected PE read circuits or functions. Also included is a description of PE read data test tape, part number 5080-4555. Knowledge o f the contents of the test tape is required to know which circuits and functions are checked when a given portion of the tape is run.

5-97. TEST EQUIPMENT REQUIRED. Test equipment required to do performance tests on the PE read circuits is listed below.

a. Control and status test PCA, part number 13191-60010.

b. Read data test PCA, part number 13196-60000.

c. Oscilloscope, HP 180A dual trace, or equivalent.

d. Phase-encoded read circuits test tape, part number 5080-4555.

e. Write formatter PCA, part number 13195-60000.

f. Write formatter test PCA, part number 13196-60001.

g. Scratch certified 3200 frpi tape.

h. Reference amplitude test tape, part number 5080-4548.

i. Master alignment tape, part number 9162-0027.

5-98. TEST TAPE, PN 5080-4555. The PE read data test tape is a 1200-foot prerecorded tape which can be used for performance testing and troubleshooting of the PE read circuits. It is divided into four sections by BOT and EOT reflective tabs.

5-99. Section 1 is a 450-foot section of nine-byte single-rotating bit pattern blocks. That is, each byte contains eight "0" data bits and one "1" data bit. The "1" data bit occurs once in each channel per block. The primary purpose of this section is to verify data recovery, data transfer, and data block detection.

5-100. Section 2 is a 100-foot section containing a 40-foot length of ID burst blocks, a 15-foot blank space and a length of file mark blocks. This section can be used to verify ID bursts and file marks.

5-101. Section 3 contains four 40-foot groups of PE data blocks in which the data of one channel is skewed a known amount. The data groups are separated by 15-foot inter-record gaps. Each block begins with a normal 41-byte preamble and is terminated with an 80-byte postamble.

This section verifies skew buffer operation. The long postamble allows verifications of postamble detection capability.

5-102. Section 3, group A is 40-feet of five-character blocks. The data pattern in channel P is 11111. The data pattern in channels zero through seven is 01010. Channel one is delayed by 1.5 byte times.

5-103. Section 3, group B is the same as group A except that channel one is delayed 2.5 byte times.

5-104. Section 3, group C is 40 feet of five-character blocks. The data pattern in channel zero is 11111. The data pattern in channels P and one through seven is 01010. Channel one is delayed by 1.5 byte times.

5-105. Section 3, group D is the same as group C except that channel one is delayed 2.5 byte times.

5-106. Section 4 is a 400-foot section containing blocks of ANSI format B data recorded while the tape speed is externally modulated, this provides a short-term average density variation of ±15 percent. Section 4 is used to check the PE read system clock's ability to synchronize to incoming data.

5-107. PE READ CIRCUITS OVERALL PERFORMANCE TESTS. This test checks the ability of the PE read circuits to generate each output signal when the proper conditions exist. It is, therefore, an overall performance test of the PE read circuits. To perform the test, proceed as follows:

a. On tape units with a density select switch on the front panel, select 1600.

b. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

c. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the loadpoint of section 1.

d. Use the CF switch on the control and status test PCA (13191-60010) to set the tape in forward motion and check that the RC, EOB, and SD16 indicators on the read data test PCA are on, and the MTE, STE, IDB, and TM indicators are off.

e. Connect the oscilloscope channel A probe to the parity channel preamplifier DIFF test point and adjust the sweep rate so that the block occupies 8 cm. Connect the channel B probe to the EOB test point on the read display test PCA. A single pulse should be present within ±0.3 cm of the 10 cm line (approximately 22 to 24 byte times from the end of the data block).

f. Connect the channel B oscilloscope probe to the RC test point on the read data test PCA. Adjust oscilloscope sweep as necessary to verify that nine $\overline{RC}$ pulses occur for each zero volts line crossing of the signal of channel A. The $\overline{RC}$ pulse should be a negative pulse with a duration of 2.5 ± 0.5 microseconds.

g. Connect the trace A oscilloscope probe to the P data bit test point on the read data test PCA. Adjust the oscilloscope so that the spacing between the $\overline{RC}$ pulses is 1 cm and the negative-going edge of the $\overline{RC}$ pulse is at the first oscilloscope graticule line. The waveform at the P test point should be a negative pulse one cm wide. It should begin at the same time as the $\overline{RC}$ pulse and be active (low) during the first cm on the graticule.

h. Connect the channel A oscilloscope probe to the read data test PCA test points for data channels zero through seven in turn. The pulse present at test points 0 through 6 should be the same as for test point P except that the channel zero pulse appears on the second cm of the graticule, the channel one pulse appears

on the third cm, etc. The channel seven pulse should go low and remain low until the EOB pulse occurs.

i. Set the tape in reverse motion and check that the RC and EOB indicators on the read data test PCA are on, and the MTE, STE, and EVEN indicators are off.

5-108. SKEW BUFFER OVERFLOW DETECTION. This test checks the ability of the error detection circuits to detect a skew buffer overflow.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Use the CF switch on the control and status test PCA to set the tape in forward motion and, temporarily, short the DRDY test point on the master PE read control PCA to ground. The STE and MTE indicators on the read data test PCA should light.

5-109. STE VERIFICATION. This test checks the threshold detector, low amplitude detector, and error detection circuits on the decoder PCA for each channel, the TIE decoder logic, and the single-track error and multiple-track error circuits in the state control logic. These circuits should light the STE indicator when a single track error is simulated on any channel. Also, the MTE indicator is checked to see that it does not light erroneously under single-track error conditions.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Use the CF switch on the control and status test PCA to set the tape in forward motion, then temporarily short the DIFF test point, on the preamplifier PCA for channel P, to ground. The STE indicator on the read data test PCA should light and the MTE indicator should remain off (although it may flicker while the ground connection is made).

e. Repeat step d for channels zero through seven.

5-110. MTE VERIFICATION. This test verifies that the threshold detector, low amplitude detector, and error detection circuits on the decoder PCA for each channel and the TIE decoder logic and the MTE circuit in the state control logic are capable of detecting a low amplitude condition of the input signal from the preamplifier on two channels. Also, the ability of the TIE decoder logic and MTE circuit to discriminate between a single-track error and a multiple-track error is checked.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Short the DIFF test point on the P channel preamplifier to ground.

e. Use the CF switch on the control and status test PCA to set the tape into forward motion and temporarily short the DIFF test point on the zero channel preamplifier to ground. The MTE indicator on the read test PCA should be on only while both DIFF test points are grounded.

f. Repeat step e for channels one through seven, in turn.

5-111. EVEN SIGNAL AND READ ONLY STATES PERFORMANCE TEST. This test checks that the error correction circuits generate an active $\overline{\text{EVEN}}$ signal when the required conditions exist. It also checks that the state control logic passes through all read-only states (00, 01, 03, 07. 17, 12, 02, 16, 13, and 11) while reading a data block. This is done by determining that the $\overline{\text{RC}}$ signal becomes active during reading of each data block. Since the $\overline{\text{RC}}$ signal is initiated in state 02, $\overline{\text{RC}}$ signals occurring in two successive blocks indicate the state control logic has passed from state 00, through the data loop (states 17, 12, 02, and 16), to state 11.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Short the LSB test point for the P channel decoder PCA to ground and use the CF switch on the control and status test PCA to set the tape into forward motion. The EVEN and MTE indicators on the read data test PCA should light.

e. Connect one oscilloscope probe to the RC test point on the read data test PCA. Connect the other oscilloscope probe to the DIFF test point on the P channel preamplifier and verify that two $\overline{RC}$ pulses occur for each block.

f. Remove the short on the P channel LSB test point and short, to ground, the LSB test point on the decoder PCA for each of channels zero through seven, in turn. For each channel, the EVEN and MTE indicators should light but only one $\overline{RC}$ pulse should occur per block.

5-112. FALSE PREAMBLE DETECTION PERFORMANCE TEST. This test checks that the state control logic will detect an improper preamble while passing through states 00, 04, and 05 in read-after-write mode.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 1.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Short the DIFF test point on the P channel preamplifier PCA to ground and set the tape into forward motion. The STE indicator on the read data test PCA should light.

e. With the P channel DIFF test point shorted, short the LWRITE test point on the data and status PCA to grounnd. The STE and MTE indicators on the read data test PCA should be on and the RC indicator should be off.

5-113. ID BURST DETECTION PERFORMANCE TEST. This test checks that the state control logic passes through the proper states (00, 01, 03, 13, and 11) when supplied an identification burst in read only mode.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit and position the tape at the load point of section 2.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Short the DIFF test point on the channel P preamplifier to ground and set the tape in forward motion. The IDB indicator on the read data test PCA should not light, the EOB indicator should light at the end of each block, and the RC and

MTE indicators should be off.

5-114. TM DETECTION PERFORMANCE TEST. This test checks that the state control logic passes through the proper states (00, 01, 03, 13, and 11) when supplied a tape mark in read-only mode (step d). It also checks that a tape mark will not be detected if a faulty tape mark is supplied (steps e and f).

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Set the tape at the beginning of the tape mark part of section 2 of the test tape and set the tape in forward motion. The TM and EOB indicators on the read test PCA should be on. The RC, MTE, and STE indicators should be off.

e. Short the DIFF test point on the channel two preamplifier to ground. Bring the tape to the beginning of the tape mark part of section 2 and set the tape in forward motion. The TM indicator on the read data test PCA should remain off and the MTE indicator should be on.

f. Repeat step e, shorting the DIFF test point on the channel six preamplifier instead of the channel two preamplifier. Again, the TM indicator should remain off and the MTE indicator shoud be on.

5-115. SKEW CORRECTION PERFORMANCE TEST. This test verifies the ability of the decoder PCA skew buffers to correct skew. Steps d, e, and h of this test supply the channel one skew buffer with a signal which lags the signals in the other channels by 1.5 byte times. The skew buffers of the other channels should store the data for the first two bytes until the first data bit for channel one is stored in the channel one skew buffer. Step d checks skew buffer operation while the tape is running forward. Step e performs the same check with the tape running in reverse, thus also checking that the zero crossing enable logic is inverting the input signal in reverse mode.

The sections of tape used in steps d through g have identical data patterns in every channel (five data bits with the pattern 01010) except the parity channel which has a 11111 pattern (five data bits also). Steps h and i use sections of the tape which has an identical pattern (five data bits with the pattern 01010) in every channel except the zero channel which has a 11111 pattern.

Steps f, g, and i perform the same tests as steps d, e, and h, respectively, except that the channel one signal lags the others by 2.5 byte times instead of 1.5 byte times.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Bring the tape to the beginning of part A of section 3. Set the tape into forward motion and observe the indicators on the read data test PCA while reading a short section of the tape, then stop tape motion. The RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should stay off.

e. Set the tape into reverse motion and read the same portion of tape as in step a. Again, the RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should remain off.

f. Bring the tape to the beginning of part B of section 3. Set the tape into forward motion, observe the indicators on the read data test PCA while reading a short section of the tape, then stop tape motion. The RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should stay off.

g. Set the tape into reverse motion and read the same portion of tape as in step f. Again, the RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should remain off.

h. Bring the tape to the beginning of part C, section 3. Set the tape into forward motion, observe the indicators on the read data test PCA while reading a short section of the tape, then stop tape motion. The RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should stay off.

i. Bring the tape to the beginning of part D, section 3. Set the tape into forward motion, observe the indicators on the read data test PCA while reading a short section of the tape, then stop tape motion. The RC and EOB indicators should be on and the STE, MTE, and EVEN indicators should stay off.

5-116. FALSE POSTAMBLE DETECTION PERFORMANCE TEST. This test checks that a false postamble will be detected by the state control logic in state 15. Steps d through g perform this check for read-only mode. Steps h and i perform the check for read-after-write mode. In the read only mode check, the state control logic passes through states 00, 01, 03, 07, 17, 12, 02, 16, 15, 13, and 11. In the read-after-write mode check, the state control logic passes through states 00, 04, 05, 07, 17, 12, 02, 16, 15, 13, and 11.

The taped data produces a false $\overline{\text{EOD}}$ signal to set the state control logic into state 15 (the postamble verification state) on the second data byte. In state 15, the fact that the $\overline{\text{SBEZ}}$ signal is not active on the third byte (because the third byte contains data) will produce an active $\overline{\text{MTE}}$ signal.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555 in the tape unit.

c. Install the following PCA's in the tape unit under test.

(1) Control and status PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Bring the tape to the beginning of part A, section 3. (Use only part A for this test. Do not over-run into part B).

e. Short the DIFF test point on the P channel preamplifier to ground and set the tape into forward motion. The STE, MTE, EOB, and RC indicators on the read data test PCA should be on and the EVEN indicator should be off.

f. Remove the short from the P channel DIFF test point and short the DIFF test point on the channel zero preamplifier to ground.

g. Set the tape into forward motion. The RC, STE, and EOB indicators on the read data test PCA should light and both the EVEN and MTE indicators should remain off.

h. Bring the tape to the beginning of part A of section 3.

i. Short the LWRITE test point on the data and status PCA to ground and set the tape into forward motion. The MTE, and EOB indicators on the read data test PCA should light. The EVEN, RC, and STE indicators should remain off.

5-117. CLOCK SYNCHRONIZATION PERFORMANCE TEST. This test checks the clock and clock control logic synchronization function while reading a section of tape with a short-term density variation of ±15 percent. Step d checks the ability of the clock to keep synchronized to the incoming data. Steps e and f check that the clock control logic will synchronize the clock to the parity channel Sync Pulse when the channel two Sync Pulse is disabled. Step g checks that the clock control logic causes the clock to operate at its fixed frequency in read-after-write mode.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Bring the tape to the beginning of section 4. Set tape into forward motion and read the tape for at least 30 seconds. The RC and EOB indicators on the read data test PCA should light and the STE and MTE indicators should remain off.

e. Bring the tape to the beginning of section 4 and short the DIFF test point on the channel two preamplifier to ground.

f. Set the tape into forward motion and read the tape for at least 30 seconds. The STE indicator on the read data test PCA should light and the MTE indicator should remain off.

g. Remove the short from the channel two DIFF test point and short the LWRITE test point on the data and status PCA to ground. Set the tape into forward motion. The MTE indicator should alternate between an on and off condition.

5-118. STATUS LOGIC PERFORMANCE TEST. This test checks the portion of the status logic which controls the $\overline{SD16}$ and the MREV signals. The other signals generated by the status logic are checked by other performance tests. Steps d through h check the logic which generates the $\overline{SD16}$ signal. Step i checks the MREV signal as initiated by the $\overline{REV\ 1}$ signal from a slave unit.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

c. Install a scratch tape in the tape unit.

d. With the tape unit selected and on line (a high present at TP3 on control and status PCA) and the tape stopped, check that the SD16 indicator on the read data test PCA is on.

e. Disconnect the unit select jumper on control and status test PCA (13191-60010). This de-selects the tape unit, and the SD16 indicator should be off. Reconnect the jumper.

f. If the tape unit has an 800 density switch, select 800 density; then select 1600 density. The SD16 indicator should be off while 800 density is selected.

g. Place the tape unit off line by pressing the RESET pushbutton on the tape unit front panel. The SD16 indicator should be off.

h. With the tape unit still off line, short pin 24X at connector J16 on the master PE read motherboard to ground. The SD16 indicator should be on while the pin is shorted to ground.

i. Set the tape into forward motion and short pin 23X to ground at slave connector J16 on the PE master motherboard. The MTE indicator on the read data test PCA should light while the short is in place.

j. Remove shorts to ground installed in steps "h" and "i".

5-119. PE READ PREAMPLIFIER GAIN PERFORMANCE TEST (READ-ONLY UNITS). Before performing the following procedures, ensure that the tape transport long-term speed variation is within specification. To check the preamplifier gain, proceed as follows:

a. Install reference amplitude test tape, part number 5080-4548, in tape unit.

b. If the tape unit under test has 1600 density select switch on front panel, select 1600.

c. Connect oscilloscope probe to DIFF test point on the read preamplifier PCA for the parity channel (PE test point on seven/nine-track tape units).

d. Set tape into forward motion at synchronous speed and observe waveform. Average peak-to-peak amplitude should be 4.0 $\pm$ 0.3 volts.

e. Repeat steps c and d for each of the remaining channels (zero through seven).

5-120. PE READ PREAMPLIFIER GAIN PERFORMANCE TEST (READ/WRITE UNITS). Before performing the following procedures, ensure that the tape transport long-term speed variation is within specification. To check the preamplifier gain of read/write units, proceed as follows:

a. Install a scratch certified 3200 frpi tape in tape unit.

b. Install control and status test PCA, part number 13191-60010, PE write formatter, part number 13195-60000, and write formatter test PCA, part number 13195-60001 in the tape unit.

c. Connect oscilloscope probe to DIFF test point of read preamplifier for parity channel.

NOTE: A feed-through signal from the write head will be observed riding on the test point signal. The limits indicated in the following step refer to portions of the test point signal which are free of obvious write head feed-through distortion.

d. Use test PCA's listed in step b to write continuous 1600 frpi in all nine tape channels. While writing, measure average peak-to-peak amplitude of the pre-amplifier signal at test point. Peak-to-peak amplitude should be 4.5 $\pm$ 0.3 volts.

e. Adjust oscilloscope to display several cycles of test point signal. Waveforms should be free of clipping and discontinuities (ignore write head feed-through signals).

f. Repeat steps c through e for each of the eight remaining channels.

5-121. PE THRESHOLD LEVEL PERFORMANCE TEST (READ-ONLY UNITS). To check the threshold level of a PE master read-only tape unit, proceed as follows:

a. Install a scratch tape in the tape unit.

b. Connect the common (ground) lead of a dc voltmeter, with an accuracy of one percent or better, to the GND test point on the PE data and status PCA (master units) on the GND test point on the PE slave read PCA (slave units).

c. Set tape unit into forward tape motion and use voltmeter to check voltage at +THR and -THR test points on PE data and status PCA. They should be as follows:

+THR: +0.30±0.02 Vdc.
-THR: -0.30±0.02 Vdc. (-THR used on 07970-62041 PCA only)

5-122. PE THRESHOLD LEVEL PERFORMANCE TEST (READ/WRITE UNITS). To check the threshold level of a PE read/write tape unit, proceed as follows:

a. Install a scratch tape in the tape unit.

b. Connect the common (ground) lead of a dc voltmeter, with an accuracy of one percent or better, to the GND test point on the PE data and status PCA (master units) or the GND test point on the PE slave read PCA (slave units).

c. Connect TP1 (WSW signal) of the control and status PCA to GND.

d. Set tape unit into forward tape motion and use voltmeter to check voltage at +THR and -THR test points on PE data and status PCA. They should be as follows:

+THR: +0.77±0.02 Vdc.
-THR: -0.77±0.02 Vdc. (-THR used on 07970-62041 PCA only)

5-123. STATIC SKEW PERFORMANCE TEST. Before performing the following test, ensure that the tape transport is operating properly. To check the static skew, proceed as follows:

a. Install master alignment tape, part number 9162-0027, in tape unit.

NOTE: Waveforms for a slave unit can be monitored at the DAT test points on the read decoder PCA's in the master unit, provided the slave unit is connected to the master unit and selected on the master unit select switch. If the slave unit is not connected to the master unit, monitor the waveforms at the test points on connector P2 of the slave read PCA. The test point for master units is the DAT test point on the read decoder PCA.

b. Connect oscilloscope channel A probe to DAT test point on read decoder PCA for the parity channel.

c. Connect oscilloscope channel B probe to DAT test point on the read decoder PCA for channel two. (Channel two is used as the reference channel).

d. Set tape unit for synchronous speed forward and adjust oscilloscope sweep to trigger on positive edge of whichever waveform goes positive first. (If parity channel waveform goes positive before channel two waveform, trigger oscilloscope sweep on parity channel waveform; otherwise trigger oscilloscope sweep on channel two waveform).

e. Adjust oscilloscope for alternate display of channels A and B.

f. Estimate and record average time difference between positive edges of waveforms. Also, record whether parity channel waveform occurs before or after channel two waveform.

g. Repeat steps b and d through f for channels zero, one, and three through seven. Leave oscilloscope channel B connected to channel two (reference channel).

h. Add largest time difference by which a waveform precedes channel two waveform plus largest time difference by which a waveform follows channel two waveform.

i. Multiply sum of largest leading and lagging time differences (in microseconds) by tape speed (in inches/second) to obtain static skew in microinches. Skew should be less than 300 microinches.

5-124. PHASE ENCODED WRITE CIRCUITS PERFORMANCE TESTS.

Performance tests on the PE write circuits consist of an overall performance test and tests for uncompensated write skew, erase phasing, assymmetry of write time for each data bit, crosstalk from the write heads to the read heads, and efficiency of the erase heads.

5-125. TEST EQUIPMENT. Test equipment required to check performance of the PE write circuits is as follows:

a. Control and status test PCA, part number 13191-60010.

b. Read data test PCA, part number 13196-60000.

c. Write formatter PCA, part number 13195-60000.

d. Write formatter test PCA, part number 13196-60001.

e. Oscilloscope, HP 180A dual trace, or equivalent.

f. Scratch certified 3200 frpi tape.

5-126. OVERALL WRITE PERFORMANCE TEST. The following test is useful for checking the write capability of the write circuits. However, since the master PE read circuits are used as test equipment in this test, it is necessary that they be operating correctly.

NOTE: If the tape unit under test is a slave unit, it will be necessary to connect it to the master unit to perform this test.

a. Install the following test PCA's in the master tape unit:

(1) Control and status test PCA, part number 13191-60010.

(2) Write formatter PCA, part number 13195-60000.

(3) Write formatter test PCA, part number 13196-60001.

b. Install the read data test PCA, part number 13196-60000 in the unit under test.

c. Install a scratch tape in the tape unit under test and bring it to the load point.

d. On the write formatter test PCA, set the switches as follows:

SWITCH	POSITION
DATA SELECT	SINGLE ROTATING BIT
END OF DATA	Right position
DATA BLOCKS	Left position
WRITE ID BURST	Left position
TAPE MARK	Left position
Thumb Wheel Variable Resistor	fully counterclockwise

e. On the write formatter PCA, make sure the speed jumper is set to the speed of the unit under test and the parity jumper is set to the odd parity position.

f. On the control and status test PCA, select WSW.

g. Press the ON LINE switch on the tape unit front panel, then set the tape into forward moton using the CF switch on the control and status test PCA. The SD16 indicator on the read data test PCA should be on and the RC and EOB indicators should be off.

h. Set the DATA BLOCKS switch on the write formatter test PCA to the right position. The RC and EOB indicators should flash, the EVEN, STE, and MTE indicators should remain off, the P channel should be on bright, and the remaining channel indicators should be on dim.

5-127. UNCOMPENSATED WRITE SKEW PERFORMANCE TEST. This test measures the amount of write skew before it is adjusted out using the skew adjustment variable resistors on the write data PCA's.

a. Install a write enable ring on the tape reel.

b. Install a scratch tape in the tape unit and bring it to the load point.

c. On tape units with a density select switch on the front panel, select 1600.

d. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Write formatter PCA, part number 13195-60000.

(3) Write formatter test PCA, part number 13196-60001.

e. Use the test PCA's to write continuous 1600 frpi on all channels while monitoring the waveform at the ODD CHANNEL SKEW test point on the single-channel write data PCA. Note the width of the positive pulse present there. It should be less than 290/V microseconds, where V is the transport synchronous speed in inches per second.

f. Repeat step e for the ODD CHANNEL SKEW and EVEN CHANNEL SKEW test points on all remaining write data PCA's.

g. Subtract the shortest reading from the longest reading and multiply the difference by V. This is the uncompensated write skew in microinches. It should be less than 250 microinches.

5-128. ERASE PHASING PERFORMANCE TEST. This performance test need be performed only after installing a new or reconditioned head assembly.

a. Install a write enable ring on the tape reel.

b. Install a scratch tape in the tape unit and bring it to the load point.

c. On tape units with a density select switch on the front panel, select 1600.

d. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Write formatter PCA, part number 13195-60000.

(3) Write formatter test PCA, part number 13196-60001.

e. Select manual mode (PROG/MAN switch) on the control and status test PCA.

f. Use the WSW switch on the control and status test PCA to deactivate the WSW signal to the tape unit.

g. Use the WSW switch on the control and status test PCA to activate the WSW signal.

h. Set all switches on the write formatter test PCA to the left position. Then, with the END OF DATA switch in the left position, momentarily set it to the right position. (This sets the write head flip-flops on the write data PCA's to the reset flux (erase) condition).

i. Use the CF switch on the control and status test PCA to produce approximately 25 feet of forward tape travel. (This erases 25 feet of tape).

j. Use the REW/SET-REW switch on the control and status test PCA to rewind the tape to the load point.

k. Select programmed mode on the control and status test PCA (MAN/PROG switch) and activate the CF switch to initiate the start-stop tape movements. At the same time, use the WSW switch to repeatedly activate and deactivate the $\overline{WSW}$ signal. (This creates written and unwritten portions of the tape). Continue for 25 feet, then stop.

l. Deactivate the $\overline{WSW}$ signal and select manual mode on the control and status test PCA, then rewind the tape to the load point.

m. Connect the oscilloscope probe to the DIFF test point on the channel P read preamplifier and set the tape into forward motion using the CF Switch on the control and status test PCA. Spikes present at the test point should be less than $\pm$0.25 volt.

n. Repeat steps m and n for each of channels zero through seven.

5-129. WRITE TIME ASSYMMETRY PERFORMANCE TEST. This test checks that write time is the same for each data bit.

a. Install a write enable ring on the tape reel.

b. Install a scratch tape in the tape unit and bring it to the load point.

c. On tape units with a density select switch on the front panel, select 1600.

d. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Write formatter PCA, part number 13195-60000.

(3) Write formatter test PCA, part number 13196-60001.

e. Set the DATA SELECT switch on the write formatter test PCA to write 1600 frpi.

f. If the tape unit under test is a master unit, connect the scope probe to the DAT test point on the channel P decoder PCA. If it is a slave unit, either connect it to the master and use the DAT test point or connect the scope probe to pin 1X on slave PE read assembly connector RSJ1.

g. Use the CF switch on the control and status test PCA to set the tape into forward motion and adjust the oscilloscope carefully so that one period of the waveform occupies 10 cm on the scope. The waveform transitions will exhibit some jitter. Use the center of the jitter band as the transition position. The mid-period transition should be within $\pm$0.2 cm of the center (5 cm) line. (This is $\pm$4 percent asymmetry).

h. Repeat step g for channels zero through seven. The slave test points are as follows:

CHANNEL	RSJ1 PIN
0	3X
1	5X
2	7X
3	9X
4	11X
5	13X
6	15X
7	17X

5-130. WRITE CROSSTALK PERFORMANCE TEST. This test measures the crosstalk from the write heads to the read heads during read-after-write mode.

a. Install a write enable ring on the tape reel.

b. Install a scratch tapein the tape unit and bring it to the load point.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Write formatter PCA, part number 13195-60000.

(3) Write formatter test PCA, part number 13196-60001.

d. On the write formatter test PCA, set the DATA SELECT switch for 1600 frpi.

e. Activate the $\overline{\text{WSW}}$ signal using the WSW switch on the control and status test PCA. Then use the CF switch on the control and status test PCA to start, then stop, forward tape motion. (Under these circumstances, write data and write clock signals are being supplied to the heads even though the tape is stationary).

f. Connect the oscilloscope probe to the DIFF test point on the channel P read preamplifier and measure the amplitude of the signal present there. It should be less than 0.5 volts.

g. Repeat step f for all channels.

5-131. ERASE HEAD EFFICIENCY PERFORMANCE TEST. This test checks the noise level of tape which has been erased by two methods; erasing with both the erase head and the write head and erasing using the erase head alone.

a. Install a write enable ring on the tape reel.

b. Install a scratch tape in the tape unit and bring it to the load point.

c. On tape units with a density select switch on the front panel, select 1600.

d. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA , part number 13191-60010.

(2) Write formatter PCA, part number 13195-60000.

(3) Write formatter test PCA, part number 13196-60001.

e. Set the DATA SELECT switch on the write formatter test PCA to 1600 frpi.

f. Connect the oscilloscope probe to the DIFF test point on the channel four read preamplifier.

g. On the control and status test PCA, use the WSW switch to activate the $\overline{\text{WSW}}$ signal and use the CF switch to set the tape into forward motion. Adjust the oscilloscope to display 10 to 20 periods of the waveform. Write approximately 100 feet of tape.

h. Use the CR switch on the control and status test PCA to rewind the tape to the load point.

i. Remove the write formatter PCA and write formatter test PCA from the tape unit.

j. Use the CF switch to set the tape into forward motion and run approximately one-half of the 100 feet of tape written with 1600 frpi in step g. Use the oscilloscope to measure the average peak-to-peak noise at the DIFF test points on the read preamplifiers for channels four and five. Note the value for each channel.

k. Remove the write data PCA for channels four and five from the tape unit. (This disables the write head for channels four and five).

l. Again, (without rewinding) set the tape into forward motion and measure the average peak-to-peak noise at the DIFF test points on the read preamplifiers for channels four and five. It should be less than 50 millivolts peak-to-peak. (If the "erase head only" reading is greater than the "erase and write head" reading, it should not be more than 50 millivolts greater).

5-132. NRZI CIRCUITS PERFORMANCE TESTS.

Performance testing of the NRZI circuits consists of preamplifier gain checks for both seven-track and nine-track operation, a read threshold level check, a check of the head static skew, a check of the static skew after adjustment of the skew delay variable resistor on the NRZI read data PCA's to compensate for head static skew, and a check of the read character gate, strobe, and read clock signals.

5-133. TEST EQUIPMENT REQUIRED. Test equipment required for performance tests on the NRZI circuits is listed below.

a. Control and status test PCA, part number 13191-60010.

b. Oscilloscope, HP 180A dual trace, or equivalent.

c. Master alignment tape, part number 9162-0027.

d. Reference amplitude test tape (200 density), part number 5080-4547.

e. A tape of NRZI data blocks which is known to be error free.

5-134. NRZI CIRCUITS OVERALL PERFORMANCE TEST. This test is an overall performance test to determine if all NRZI circuits operate without errors. The test is performed by using the NRZI read test PCA to check for parity errors while running any tape of NRZI data blocks which is known to be error free. (The master alignment test tape, part number 9162-0027 and the reference amplitude test tape, part number 5080-4547 cannot be used because they are not written with normal NRZI data blocks). If a parity error occurs, the problem must be in the tape unit NRZI circuits (because the test tape is assumed to be without errors and the NRZI read test PCA is assumed to be operating correctly). To perform the test, proceed as follows:

a. Install the control and status test PCA and the NRZI read test PCA in the tape unit (see figure 1-3).

b. Install any tape of NRZI data blocks, which is known to be error free, in the tape unit.

c. Set all switches on the control and status test PCA to the off (down) position.

d. On the tape unit front panel, select the density of the NRZI data written on the test tape then press the ON LINE pushbutton.

e. On the NRZI read test PCA, set the following switches to the positions listed as follows:

SWITCH	POSITION
RD BL	RD BL (left)
ODD-EVEN	Select parity (odd or even) used on test tape.
HI/LO	Appropriate position (dependent on tape speed).
CYCLE/CF	CF
NORM/ERROR STOP	ERROR STOP

f. Use the CF switch on the control and status test PCA to set the tape into forward motion. If the tape stops short of the end of tape (EOT) tab, a tape unit NRZI circuit malfunction is indicated.

5-135. READ PREAMPLIFIER GAIN PERFORMANCE TEST (NINE-TRACK, NRZI). Before performing the procedures in paragraphs 5-136 through 5-140 ensure that the gain of the PE read preamplifiers is within specification. To check the gain of the nine-track, NRZI read preamplifiers, proceed as follows:

a. Install reference amplitude test tape, part number 5080-4547.

b. Select 800 density on the tape unit front panel. If the tape unit is a multiple format unit, select nine-track on the front panel multiple density switch.

c. Connect oscilloscope probe to DIFF test point on the NRZI read preamplifier for the parity channel.

d. Set tape into forward motion, at synchronous speed, and observe waveform on oscilloscope. Average peak-to-peak signal amplitude should be as called out on the label of the tape.

e. Repeat steps c and d for each remaining channel (zero through seven).

f. Adjust oscilloscope to display several cycles of waveform. Waveform should be free from evidence of clipping and discontinuities (dropout).

5-136. READ PREAMPLIFIER GAIN PERFORMANCE TEST (SEVEN-TRACK, NRZI). Before performing the procedures in paragraph 5-136 through 5-140, ensure that the gain of the PE read preamplifiers and/or the nine-track, NRZI read preamplifiers is within specification. To check the seven-track NRZI preamplifier gain, proceed as follows:

a. Install reference amplitude tape, part number 5080-4547.

b. On tape unit front panel, select seven-track and 556 density.

c. Connect oscilloscope probe to DIFF test point on the NRZI read preamplifier for the parity channel.

d. Set tape into forward motion, at synchronous speed, and observe waveform on oscilloscope. Average peak-to-peak amplitude should be as called out on the label of the tape.

e. Repeat steps c and d for each remaining channel.

5-137. NRZI READ THRESHOLD LEVEL. With no tape motion, use a digital voltmeter to check the voltage at the THR test point on the NRZI read control PCA. Reading should be +0.45 $\pm$ 0.01 volts.

5-138. READ HEAD STATIC SKEW TEST. Read head static skew is measured optically during head manufacturing and is also verified electrically on special test facilities. At this point the maximum is 150 microinches. When installed on the tape transport, certain electrical and mechanical considerations enter as factors. These may modify the static skew to a minor degree. Measurement may be used as additional information for analysis of field performance. The electronic read deskewing effectively eliminates this factor in normal operation. Measurement is as follows:

a. Use the master alignment tape, part number 9162-0027, as the source of data.

b. Connect channel A of the oscilloscope to the P (parity) preamplifier output and adjust the sweep to synchronize near the zero axis crossover on the positive slope.

c. Channel B of the oscilloscope will be connected to the various skew test points on the read cards. Channels will be used in alternate mode.

d. With the delayed sweep operated under a sweep rate of 2 us/cm, adjust the delay to display the positive-going step at the start of the channel skew delay ramp on the center of the oscilloscope. This will be the zero time reference for all other measurements. Adjust channel B gain as required to obtain good resolution.

e. Without making any further adjustments to the oscilloscope time base, move the channel B probe to each skew delay test point in sequence and note its relative position to the center of the oscilloscope. Signals to the left of center are early, and may be noted as "plus" with those to the right noted as "minus" as they are later than the signal from track P.

f. When all measurements have been completed in the forward direction; the same sequence can be repeated for the reverse. It will be necessary to readjust the time delay for positioning track P to center.

g. Review data taken and determine the two tracks that are the earliest (largest plus number) and latest (largest minus number). The time differential between them (sum of the two times) converted to microinches for the tape speed involved is the read head static skew. This number should not exceed 225 microinches.

NOTE: For readings between 200 and 225 microinches, it may be wise to correct for the electronic time delay variation in the peak detection circuitry. This may be measured by repeating steps a through f except that the oscilloscope channel A probe must be connected to the preamplifier output corresponding to the skew test point on the oscilloscope channel B probe. These figures must be subtracted from the normal readings (taken with channel P as the only sync) to determine the true head skew. Under these conditions, a true head skew in excess of 200 microinches is higher than normal but will not cause any practical problems.

5-139. COMPENSATED STATIC READ SKEW TEST. Compensated static read skew is a measure of the degree to which the electronic time delays are effective in eliminating the read head static skew. The termination of each track skew delay is the fall (or negative-going trailing edge) of the positive-going ramp visible at the SKEW test points on each read PCA. With perfect compensation these will all coincide. As a matter of practical consideration this seldom happens except during the period of adjustment with a specific master alignment tape. When comparisons are made using alignment tapes other than the one used for adjustment, or where the same tape is subject to possible damage, it is not uncommon to see a time difference of several microseconds depending on tape speed. Considering only a +1 percent error in the alignment tapes and complete stability of the skew delay, there could be a difference of 25 microinches between two tapes (allowing a time difference from 2.5 microseconds at 10 ips to 0.5 microseconds at 50 ips). Evaluate compensated skew using the following procedure:

a. Use channel A of the oscilloscope for the master reference for all skew measurements. Connect probe to the skew test point for track P read card.

b. Sync the main sweep to the negative slope of channel A waveform and set sweep speed to display two bit-to-bit distances. This will result in a negative-going trailing edge at the center of the oscilloscope and another at the right side. If there is time asymmetry in the master tape (some tapes have this and some do not), there will be double trailing edges in the center of the screen with the time difference corresponding to the recorded pulse asymmetry on the tape. If this is visible, refer to the note following step e. Use the variable setting of the main sweep to position pulses as stated. This will ensure the visibility of write time asymmetry on the master tape.

c. The delayed sweep will be used to position the next sequential bit in the center of the screen. Use the internal sync, positive slope position on the delayed sweep, and adjust the trigger level for a stable waveform. The delayed sweep should be adjusted (from the ccw position) only as far as required to permit the delayed sweep to internally trigger on the next pulse.

d. Establish final positioning of the P track reference point (negative-going trailing edge) at the center of the screen by use of the sweep positioning controls. Be sure that the delayed sweep remains correctly calibrated since correct time differences in microseconds will be required. Some positioning can be done with the trigger level.

e. Use channel B of the oscilloscope and the chopped mode to observe the relative position of all other tracks. Note these positions and determine the earliest and latest tracks. The maximum difference should be 30 microinches or less. (Speed (ips) x microseconds = microinches). If readings are between 30 and 50 microinches check the read skew for the unit. If this skew results in the difference being less than 25 microinches, no adjustment should be made unless there is agreement between two master skew tapes showing that the same relative error exists between the same tracks. If this occurs it can be presumed that the unit adjustments have remained stable (read skew within ±1 percent since last adjustment), but the previous read skew adjustment was made with a bad master alignment tape.

NOTE: Skew measurements can become somewhat difficult if significant write time asymmetry exists. This asymmetry will be observed on some master alignment tapes. No special steps can be taken when reading the master alignment tape.

f. Measurement of compensated static read skew in the reverse direction may be made by the same technique (steps a through e). Evaluation of this area becomes somewhat complex, as the magnetic characteristics of the pulse waveform in the reverse direction will not necessarily be symmetrical with the forward direction waveform.

5-140. READ CHARACTER GATE, STROBE, AND READ CLOCK TEST. The read character gate is initiated by the first "1" bit to complete a read skew delay period. The fall of read skew delay provides a trigger at the "nor" line, causing it to move in a negative direction. This fall triggers the read character gate period which is nominally 46 percent of the bit-to-bit period for each density. Termination of the gate will cause the "nor" line to move in a positive direction, which does two things. It sets the data levels at the read outputs and initiates the leading edge of the read strobe pulse. The read strobe trailing edge then generates the read clock output. The strobe delay time provides an interval for the read data outputs to settle before the read clock output occurs. Measure these characteristics as follows:

a. Load the tape unit with the master alignment tape and select 800 density on the front panel density select switch.

b. Sync the scope on the NOR test point with the negative slope. Then adjust the main sweep rate so that the next negative-going edge occurs 10 division later. (Each division now is 10 percent of the bit-to-bit period).

c. Observe that the positive-going edge (end of gate) occurs at 40 to 46 percent of the bit-to-bit period. If the density select option is included, check for all three densities using appropriate clock rates and tape with the proper densities.

Strobe pulse delay and read clock relationships to data are measured as follows:

a. Generate a data pattern that will move a single bit through all data channels in sequence. This will provide a data output pattern and will exercise each read channel in terms of initiating a read strobe.

b. Connect oscilloscope channel A to the data output of any read channel using the negative sync and auto triggering mode.

c. Remove the read data connector to establish standard measurement conditions. (Various lengths of cables and associated capacity will affect measurement).

d. Set sweep speed to 0.2 microseconds/division and establish a stable pattern for the leading edge of data (for both negative and positive sync).

e. Using the alternate triggered by A mode, connect oscilloscope channel B to the read clock test point on the read control card.

f. Observe the time difference between the leading edge of data and the leading edge of clock. The clock delay must be between 0.5 and 1.5 microseconds.

g. Observe the pulse width of the read clock. This should be between 2 and 3 microseconds.

h. The read clock output should be continuous. (This verifies that read strobe is being initiated by each read channel).

5-141. WRITE CROSSTALK TEST.

Write crosstalk (or write-feedthru) is a measure of the degree to which write head currents induce read head output voltages due to tranformer action between the write and read heads. It is expressed as a percentage of the nominal read-after-write output level. Measurement is as follows:

a. Generate a random data write pattern and place tape unit in the read-after-write mode.

b. Connect oscilloscope to individual read preamplifier output test points and note the composite peak-to-peak output level (use relatively slow sweep speeds). This will be in the vicinity of 6.4 volts peak-to-peak for typical data.

c. Stop the tape unit but do not drop $\overline{\text{WSW}}$ or give a $\overline{\text{REV}}$ command. This state will allow the write data head currents to continue, provided the write clock and data are still present.

d. Again observe the peak-to-peak composite signal level present at the output of the read preamplifier. This peak-to-peak value must not exceed 5 percent (7970B 12.5 ips and higher), 8 percent (7970B lower than 12.5 ips) of the value measured for the same track in step "b". Typical crosstalk levels must not exceed:

7970B 12.5 ips and up	320 Millivolts peak-to-peak
7970B below 12.5 ips	512 Millivolts peak-to-peak

5-142. NRZI WRITE CIRCUITS PERFORMANCE TEST.

5-143. WRITE TIME ASYMMETRY TEST.

Write time asymmetryis the departure (in microinches) of the effective magnetic location of a data bit from that location which would make all sequential data bits equal distances apart. Measurement is made as follows:

a. Place unit in the read-after-write mode with all ones at 800 cpi.

b. Use channel A of oscilloscope and connect to read skew test point.

c. Sync oscilloscope sweep on negative edge and adjust oscilloscope main sweep rate so that the 10 divisions are equal to two bit-to-bit distances. When this is done, there will be a negative-going trailing edge at the beginning of the sweep and at the end of the sweep. At the center, there may or may not be double trailing edges (this is the time asymmetry). Oscilloscope is now calibrated at 250 microinches per horizontal division, or 25 microinches if the X10 magnifier is used.

d. Observe the separation that may exist between the trailing edges at the center of the oscilloscope. The maximum acceptable condition is a total separation of 75 microinches.

5-144. WRITE/READ SKEW TEST.

The static skew of the write head is adjusted by electronic skew delays and is set to duplicate the effective bit positions exhibited by the IBM master alignment tape used to check and adjust the read electronic skew delays. Prior to performing the write/read skew test, perform the read skew test described in paragraphs 5-31 through 5-35. Log the results of the read skew test and perform the following procedures:

NOTE: Skew measurements can become somewhat difficult if significant write time asymmetry exists. When writing tapes for check of write/read skew it is important that all write pulses start with the same relative flux polarities on tape. This can be assured if there is a sequence of reverse/stop/forward drive commands prior to a skew measurement. The forward command assures complete write reset conditions as the WSW line is made true.

a. Write an all "1's" tape at 800 cpi.

b. Read this tape in the read-after-write mode, and connect the channel A probe of the oscilloscope to the skew test point of the P-track read data printed-

circuit assembly. Channel A of the oscilloscope will be used as a reference.

c. Adjust the oscilloscope sweep tc synchronize near the zero axis crossover on the positive slope. Set the oscilloscope to operate in the alternate mode.

d. With the delayed sweep operated under a sweep rate of 2 microseconds/cm adjust the delay to display the positive-going step at the start of the channel P skew delay ramp on the center of the scope. This will be the zero time reference for all other measurements. Adjust channel B gain as required to obtain good resolution.

e. Without making any further adjustments to the oscilloscope time base, move the channel B probe to each track skew delay test point in sequence and note its relative position to the center of the oscilloscope. Signals to the left of center are early, and may be noted as "plus" with those to the right noted as "minus" as they are later than the signal from track P.

f. When all measurements have been completed in the forward direction; the same sequence can be repeated for the reverse. It will be necessary to readjust the time delay for positioning track P to center.

g. Review data taken and determine the two tracks that are the earliest (largest plus number) and latest (largest minus number). The time differential between them (sum of the two times) converted to microinches for the tape speed involved is the write skew.

h. Compare the write skew readings taken with read skew test results. Any specific differences represent a measure of the inability of the tape unit write functions to duplicate the master alignment tape. A normally adjusted unit should duplicate the tape within $\pm$ 1 percent of the bit-to-bit distance at 800 cpi. This corresponds to a time difference equivalent to 25 microinches, or less.

5-145. WRITE/READ PHASING AND WRITE RESET TEST.

The following checks will verify that the write and read circuitry is correctly phased and that the LRCC character will be written.

a. Arrange for a write data program that will write three characters of all "1's", three characters of all "0's", followed by a Write Reset command. This program should be repetitive and usable for continuous writing.

b. With this program input and the tape unit operated in the read-after-write mode, observe the preamplifier output test points on each track.

c. Correct phasing and operation of the Write Reset command will result in a series of three recognizable "1" bits, three "0" bits and a single "1" bit. If phasing is correct, the first bit following the "1's" will be caused by the Write Reset and should be a positive-going pulse. It is essential that there be an odd number of all "1's" characters prior to the Write Reset Command. The number of characters of all "0's" is not critical and is only to permit

positive identification of the first character to follow.

5-146. ERASE/WRITE PHASING TEST.

This test is made only on the P track, and verifies that the erase head is correctly phased with respect to the write head. Evaluation is accomplished as follows:

a. Starting at loadpoint, write a section of all "0's" data for 30 to 60 seconds, then rewind tape to loadpoint.

b. Remove the P track write data card to preclude any further possibility of the write head changing the tape flux on the P track.

c. Place tape unit in a cyclic forward drive mode ($\overline{FWD}$ true/FWD false/$\overline{FWD}$ true, etc). During this period of time (again 30 to 60 seconds) alternate periods of $\overline{WSW}$ true/WSW false by manual operation of other means. Continue all "0's" program.

d. Operation as instructed in step "c" has resulted in intervals of tape (on track P) which have been magnetized by the write head during step "a" above, and other intervals which possibly have reversed flux polarity as set by the erase head if it is incorrectly phased.

e. After completion of steps "a" through "d", connect oscilloscope channel A to the output of channel P read preamplifier, and read the section of tape in steady forward or reverse drive mode. If the erase head is incorrectly phased, the flux reversal generated will produce full pulse amplitudes of approximately 3 volts zero-to-peak. A correctly phased head will show minor pulse disturbances as the erase current is applied. These levels will generally be below 15 percent of the zero-to-peak signal level or in the vicinity of 0.4 volts zero-to-peak, maximum.

5-147. INTERNAL WRITE CLOCK DELAY AND PULSE WIDTH TEST.

Measure the internal write clock delay by the following method.

a. The tape unit may be stopped in any mode. Write clock input signals are required.

b. Connect oscilloscope channel A to the Write Clock (WC) test point on the read control card and synchronize main sweep on negative slope.

c. Connect oscilloscope channel B to the delayed Write Clock ($\overline{WCD}$) test point and using the alternate triggered by A mode, observe the time delay between the negative-going edge of the write clock and the positive-going edge of Write Clock delayed. This should be between 1 and 3 microseconds.

d. Using channel B only, sync on positive slope and observe the pulse width of the delayed Write Clock. This should be between 0.3 and 1.0 microsecond.

5-148. DATA TRANSFER CHARACTERISITCS TEST.

The following checks cover the general data transfer characteristics of the tape unit and the final sequence of the performance checkout.

5-149. TAPE INTERCHANGEABILITY. Tape interchangeability optional test is evaluated by reading a specially prepared (random length) block tape written by a computer on a tape unit which has been specifically misadjusted to cause the maximum allowable write character skew (150 microinches absolute). The tape unit should read this tape in its entirety without read errors.

5-150. TOTAL DYNAMIC SKEW. Total dynamic skew is the microinch equivalent of the time interval between the arrival of the first and last bit of any read character under worst case data conditions (read or write) using tapes written on the unit under test. Measurement is made as follows:

a. Write a test tape having a maximum variety of random data patterns.

b. Connect channel A of the oscilloscope to the NOR test point on the read control card. The negative-going waveform at this point represents the arrival of the first data bit. All other data bits in the character will also generate negative-going waveforms at this point.

c. Sync the sweep on negative slope and adjust time as required to observe the total time required for all bits to arrive at the NOR test point.

d. This time, converted to equivalent microinches at the tape speed involved, represents the total dynamic skew of any worst case single character.

e. Operate tape unit in read-after-write, read forward, and read reverse modes. Under any of these conditions, the maximum dynamic skew must not exceed 200 microinches.

NOTE: If total dynamic skew is measured at the read clock (read clock jitter) it will appear as plus or minus dynamic skew and the total jitter band (less read clock pulse width) will correspond to $\pm$200 microinches.

1-151. READ-AFTER-WRITE DATA TRANSFER. Read-after-write data transfer is evaluated by writing a program having odd parity characters. The tape unit must operate error-free in the read-after-write mode throughout a full 10-1/2 inch reel of tape. Errors that can be positively associated with defects in the tape need not negate a test. Such errors will be read in both forward and reverse drive over the same area of tape.

1-152. READ-ONLY DATA TRANSFER. The tape generated during the read-after-write test must also be read error free in both the forward and reverse directions under read-only operation.

5-153. NRZI WRITE ADJUSTMENT PROCEDURES. The only adjustment for write data electronics is the write skew delay adjustment. Write skew delay provides additional assurance that tapes written on the unit will not have more than 150 microinches of absolute skew in any data character. This figure applies to any data pattern condition and includes all factors that cause bits to be displaced from theoretical locations. Prior to performing the write skew delay adjustment ensure that power supply adjustment, capstan adjustments, and all read data adjustments have been completed and verified.

Load the tape transport with a reel of scratch tape equipped with a write enable ring. Set all write skew delay controls fully ccw. Place the unit in synchronous forward write mode and write a data pattern consisting of all "ones" at 800 cpi. Adjust the write skew delays as follows:

a. Using an oscilloscope, compare each read channel skew in a read-after-write condition to determine which channel is lagging the most.

b. Adjust the channel 2 write skew delay until channel 2 is slightly lagging the channel determined in step "a". Channel 2 will be used as a reference channel.

c. Connect the oscilloscope channel A probe to tape unit channel 2 read SKEW test point, and connect the oscilloscope channel B probe to the SKEW test point corresponding to the write data channel being adjusted. Set the oscilloscope controls to algebraically sum channels A and B. Adjust oscilloscope sweep to display at least one full bit time (leading edge of one bit to the leading edge of the next).

NOTE: Under no circumstances are any of the read skew adjustments to be changed during the write skew compensation process.

d. Adjust the skew delay variable resistor of the channel under adjustment to obtain a maximum amplitude on the oscilloscope display.

e. Repeat step "d" for all remaining channels except the reference channel (channel 2).

NOTE: For those familiar with the forgoing information in this manual, figure 5-9 will prove handy as a general guide.

5-154. TROUBLESHOOTING.

Troubleshooting procedures for the 7970B NRZI tape units have been covered in the alignment procedures and the theory of operation. Since the 7970E PE read circuitry is more involved we will expand on the PE read circuits of a master tape unit. These procedures, which enable isolation of a malfunction to a PCA, are separated into IDB, TM and data block procedures. The simplest (IDB) procedures should be performed first. If they do not isolate the problem, the TM procedures should be performed; then, if necessary, the data block procedures. However, if the problem is know to be an IDB, TM, or data block problem, only the applicable procedures need be performed. The IDB procedures are contained in figure 5-10. Figures 5-11 and 5-12 illustrate TM and data block procedures, respectively. The procedures

are performed by running the applicable portion of test tape 5080-4555 and observing the indicators on the four test PCA's. A listing of the content of the test tape can be found in paragraphs 5-97 through 5-105.

5-155. TEST EQUIPMENT REQUIRED.

a. Control and status test PCA, part number 13191-60010.

b. Read data test PCA, part number 13196-60000.

c. Write formatter PCA, part number 13195-60000 (for read-after-write units only).

d. Write formatter test PCA, part number 13196-60001 (for read-after-write units only).

e. Phase-encoded read circuits test tape, part number 5080-4555.

f. Scratch certified 3200 frpi tape (for read-after-write units only).

NOTE: The procedures illustrated in figures 5-9, 5-10, and 5-11 isolate a malfunction only to the PCA level. If isolation to a more de tailed level is desired, signal tracing can be used.

5-156. GENERAL DISCUSSION.

As a starting point for signal tracing, two test points are suggested; the MTE flip-flop or the decoder (or state control flip-flops) on the master PE read control PCA. The eight inputs to NOR gate U45 (the gate which sets the MTE flip-flop) provide a good starting point for isolating the source of MTE indications. The state signals, at the output of decoder U210, can be checked to determine if the state control flip-flops are cycling through the required states (as illustrated in figure 4-11). As an alternative to checking the decoder outputs, the four state flip-flop test points (FA, FB, FC, and FD) can be checked with an oscilloscope to determine if the proper states are occurring . However, the outputs of the state flip-flops must be converted from voltage levels to octal code. If the flip-flops are not entering the proper states, signal tracing can be started at the inputs to the decoder (or state flip-flops). If the flip-flops are cycling through the proper states, but the required output signals from the PE read circuits are not generated, the malfunctioning circuit must be between the decoder (or state flip-flops) and the point at which the signal exits from the PE read circuits.

5-157. PREPARATION OF EQUIPMENT.

To prepare the equipment for performance of the test procedures, install the test PCA as illustrated in figure 5-5, 5-6, or 5-7, install the test tape in the tape unit, and position the tape at the beginning of the section of tape to be used.

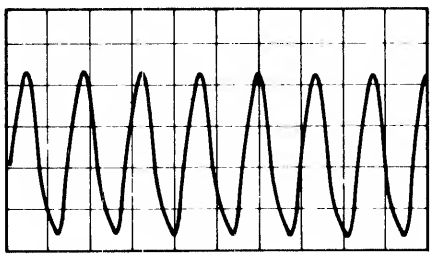
NOTE: When running a particular section of the tape, use care not to over-run into the next tape section. To do so would produce misleading indications.

Action of the indicators on the read data test PCA (such as the EOB, IDB, and TM indicators) is dependent on tape speed. At low tape speeds, the indicators which light at a certain point in the tape block will flicker when a succession of blocks are read. At high speeds, the same indicators might stay on steadily. This occurs because, at high speeds, the off time of the input signal is not sufficient to turn off the indicator.

As an added tool for further troubleshooting, refer to the available diagnostic tests.

IDB WAVEFORMS

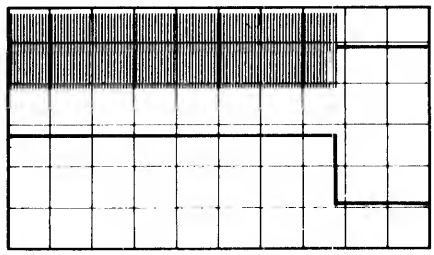
WAVEFORM 1



PE only units:
Preamplifier DIFF TP
Dual and multiformat units:
Preamplifier PE TP

Horiz = 20 µs/cm
Vert = 1.0 V/cm

WAVEFORM 2

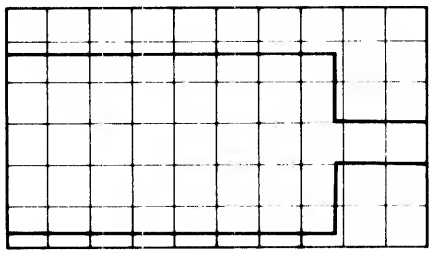


TRACE A = Parity channel preamplifier DIFF TP (PE only units) or PE TP (dual and multiformat units)

TRACE B = Parity channel decoder PCA LVL TP

Horiz = 10 ms/cm
Vert = 2 V/cm

WAVEFORM 3

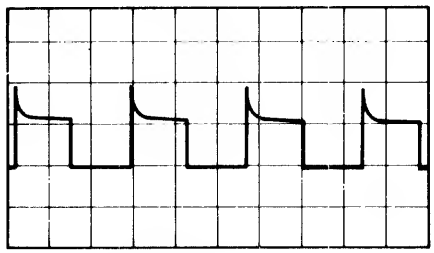


TRACE A = Parity channel decoder PCA LVL TP

TRACE B = Data and status PCA LIDL TP

Horiz = 10 ms/cm
Vert = 2 V/cm

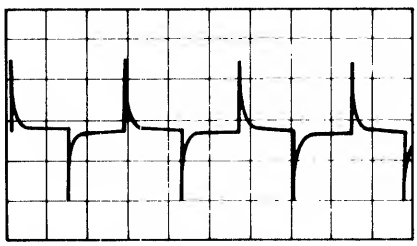
WAVEFORM 4



Write data PCA HEAD DRIVE TP

Horiz = 10 µs/cm
Vert = 10 V/cm

WAVEFORM 5



Waveform at write interconnect PCA for a typical channel.

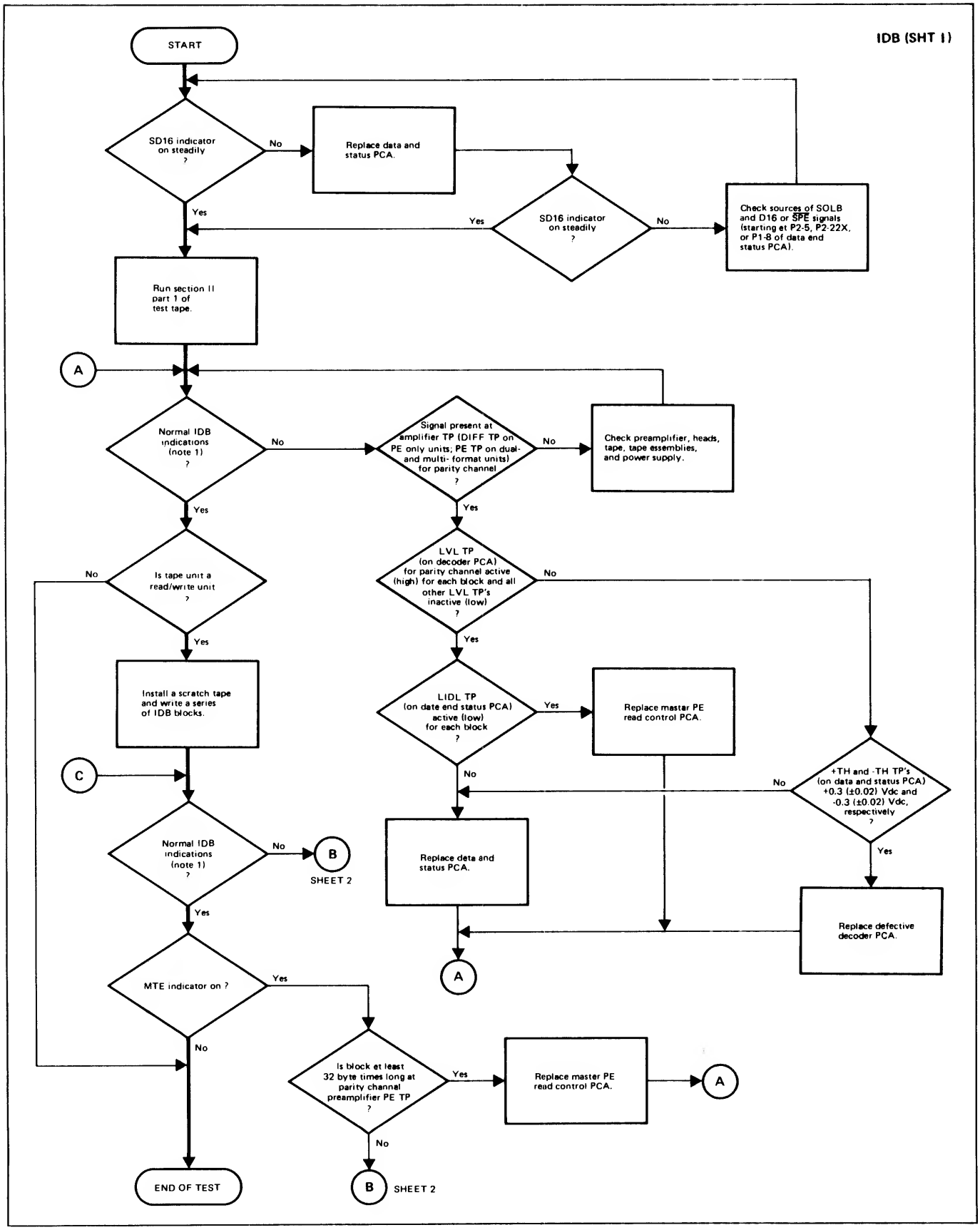
Horiz = 10 µs/cm
Vert = 5 V/cm

NOTES:

1 Normal indications, on the read data test PCA, for IDB blocks are as follows:
a. IDB indicator on for each block.
b. EOB indicator on at end of each block.
c. EOB TP active (low) at end of each block.
d. All other indicators (except SD16) off.

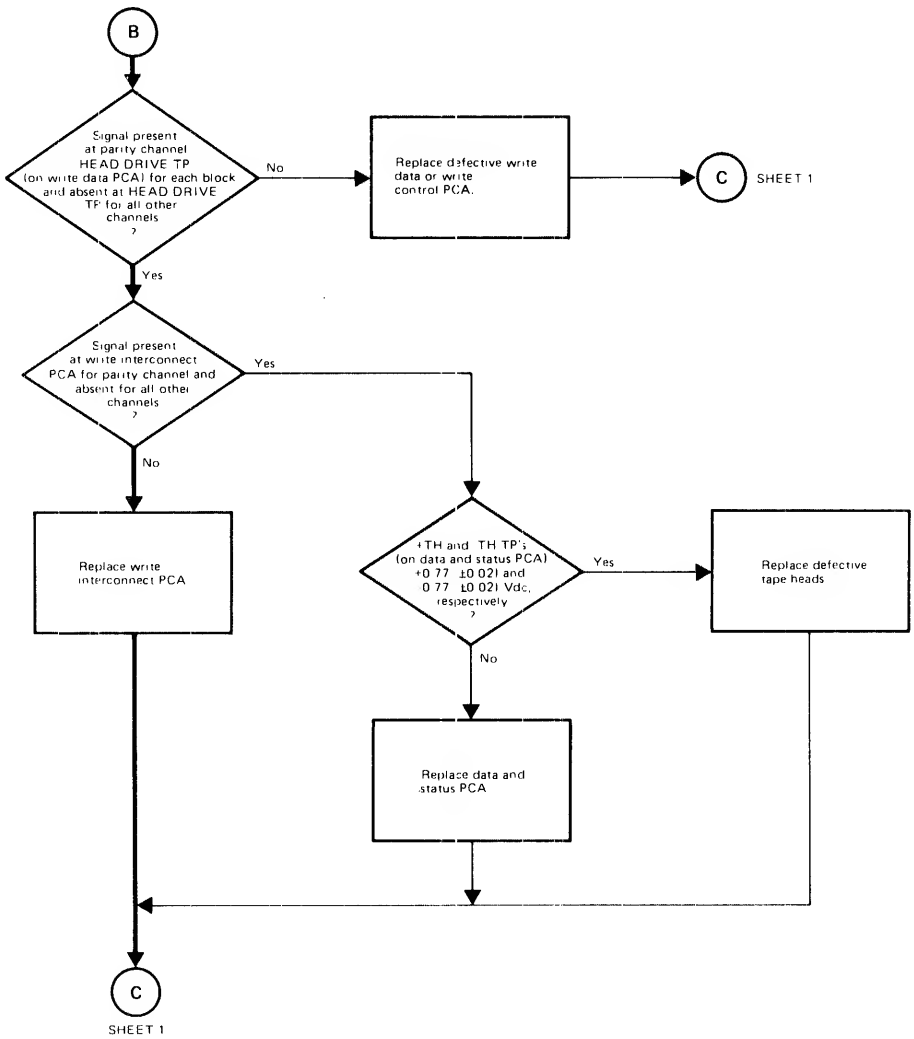
7970-543 1

Figure 5-*10.* Identification Burst Troubleshooting Flowchart (Sheet 1 of 3)



7970-543-2

Figure 5-10. Identification Burst Troubleshooting Flowchart (Sheet 2 of 3)

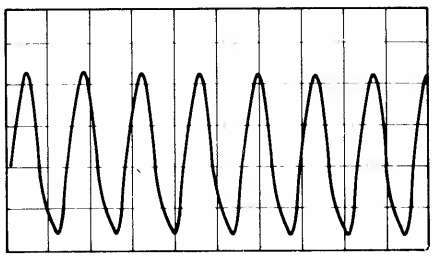


7970543-1

Figure 5-10. Identification Burst Troubleshooting Flowchart (Sheet 3 of 3)

TM WAVEFORMS

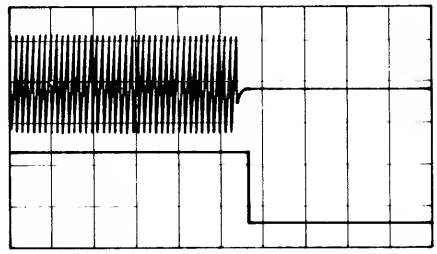
WAVEFORM 1



PE only units:
Preamplifier DIFF TP
Dual and multiformat units:
Preamplifier PE TP

Horiz = 20 μs/cm
Vert = 1.0 V/cm

WAVEFORM 2

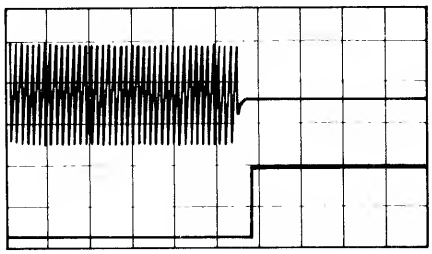


TRACE A = Channel 2 preamplifier DIFF TP (PE only units) or PE TP (dual and multiformat units)

TRACE B = Channel 2 decoder PCA LVL TP

Horiz = 0.1 ms/cm
Vert = 2 V/cm

WAVEFORM 3

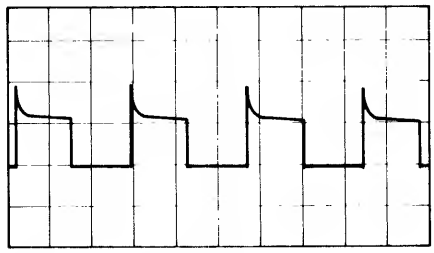


TRACE A = Channel 2 preamplifier DIFF TP (PE only units) or PE TP (dual and multiformat units)

TRACE B = Data and status PCA LTML TP

Horiz = 0.1 ms/cm
Vert = 2 V/cm

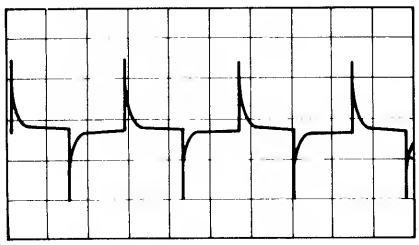
WAVEFORM 4



Write data PCA HEAD DRIVE TP

Horiz = 10 μs/cm
Vert = 10 V/cm

WAVEFORM 5



Waveform at write interconnect PCA for a typical channel

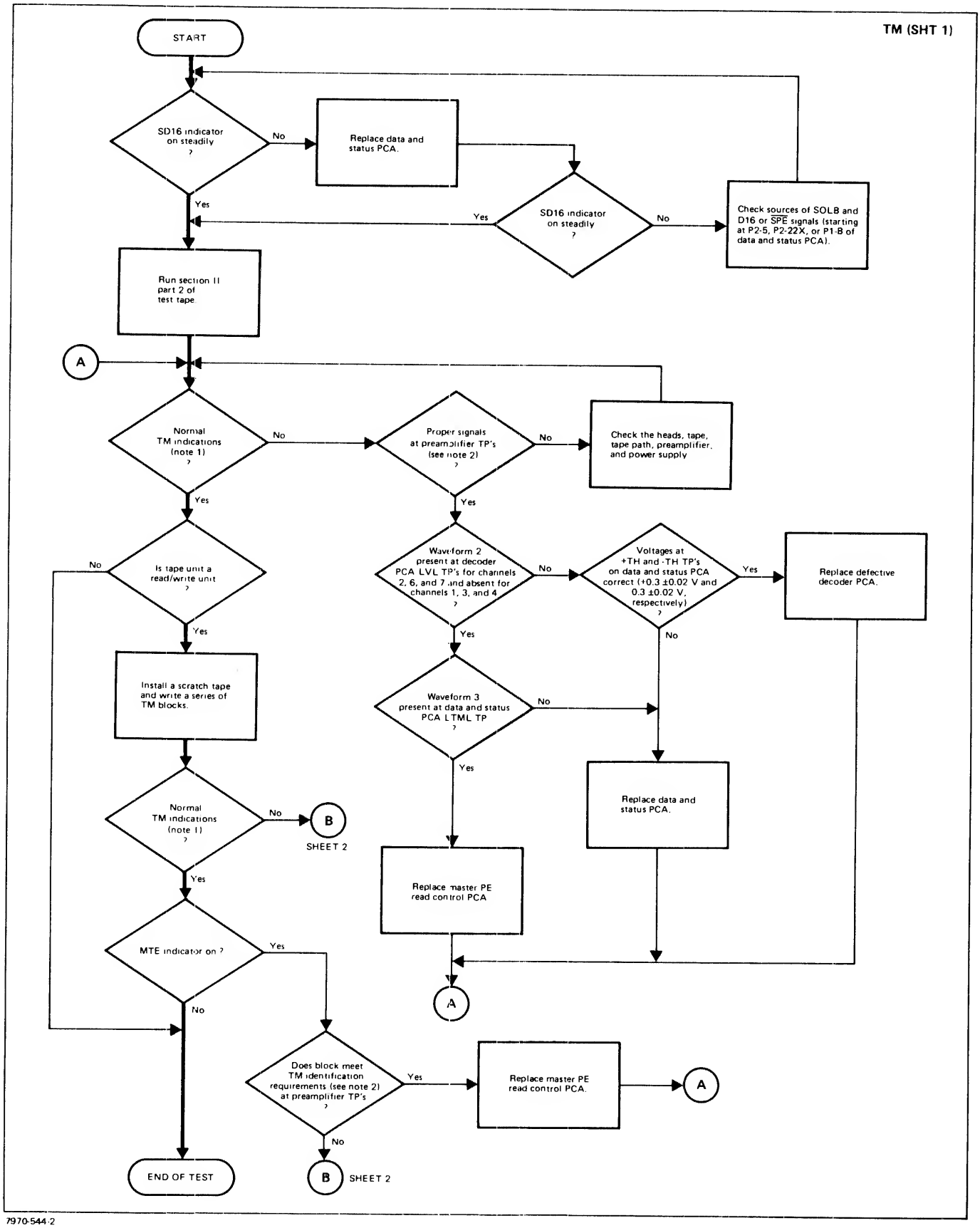
Horiz = 10 μs/cm
Vert = 5 V/cm

NOTES:

1. Normal indications, on the read data test PCA, for TM blocks are as follows:
   a. TM indicator on for each block.
   b. EOB indicator on at end of each block.
   c. EOB TP active (low) at end of each block
   d. All other indicators (except D16) off.
2. Proper tape mark signals at the preamplifier test points consists of the presence of data signals (waveform 1) on tracks 2, 6, and 7, and absence of signals on tracks 1, 3, and 4
   The test points for PE only tape units are the preamplifier DIFF test points. For dual or multiformat tape units, the preamplifier PE test points are used.

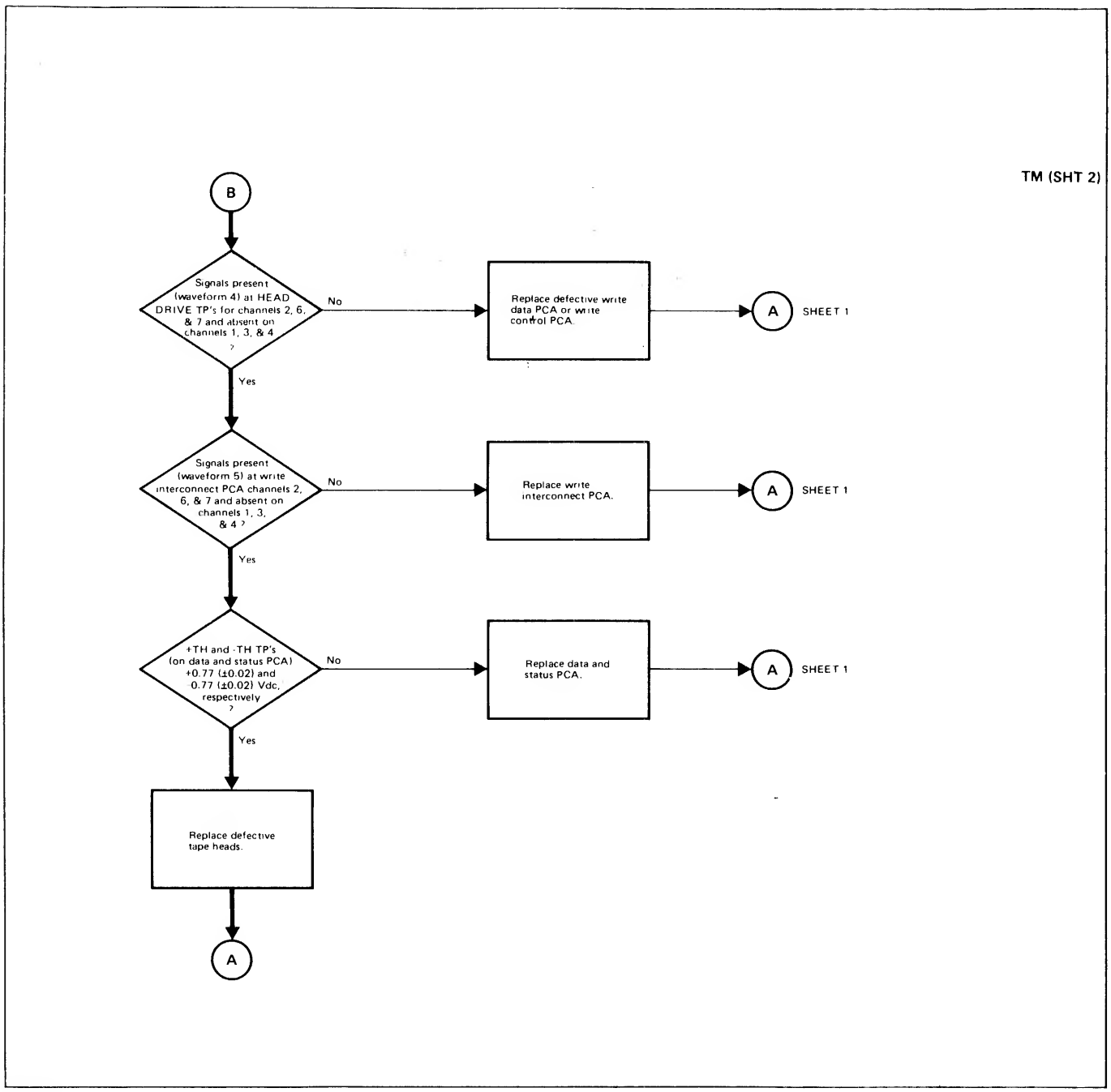
7970-544-1

Figure 5-11. Tape Mark Troubleshooting Flowchart (Sheet 1 of 3)



7970-544-2

Figure 5-11. Tape Mark Troubleshooting Flowchart (Sheet 2 of 3)

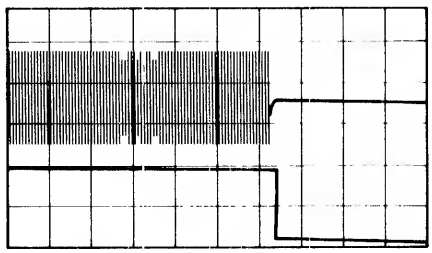


7970-544-3

Figure 5-11. Tape Mark Troubleshooting Flowchart (Sheet 3 of 3)

DATA BLOCK WAVEFORMS

WAVEFORM 1



TRACE A = Channel 2 preamplifier DIFF TP (PE only units)
or PE TP (dual and multiformat units)

TRACE B = Channel 2 decoder PCA LVL TP

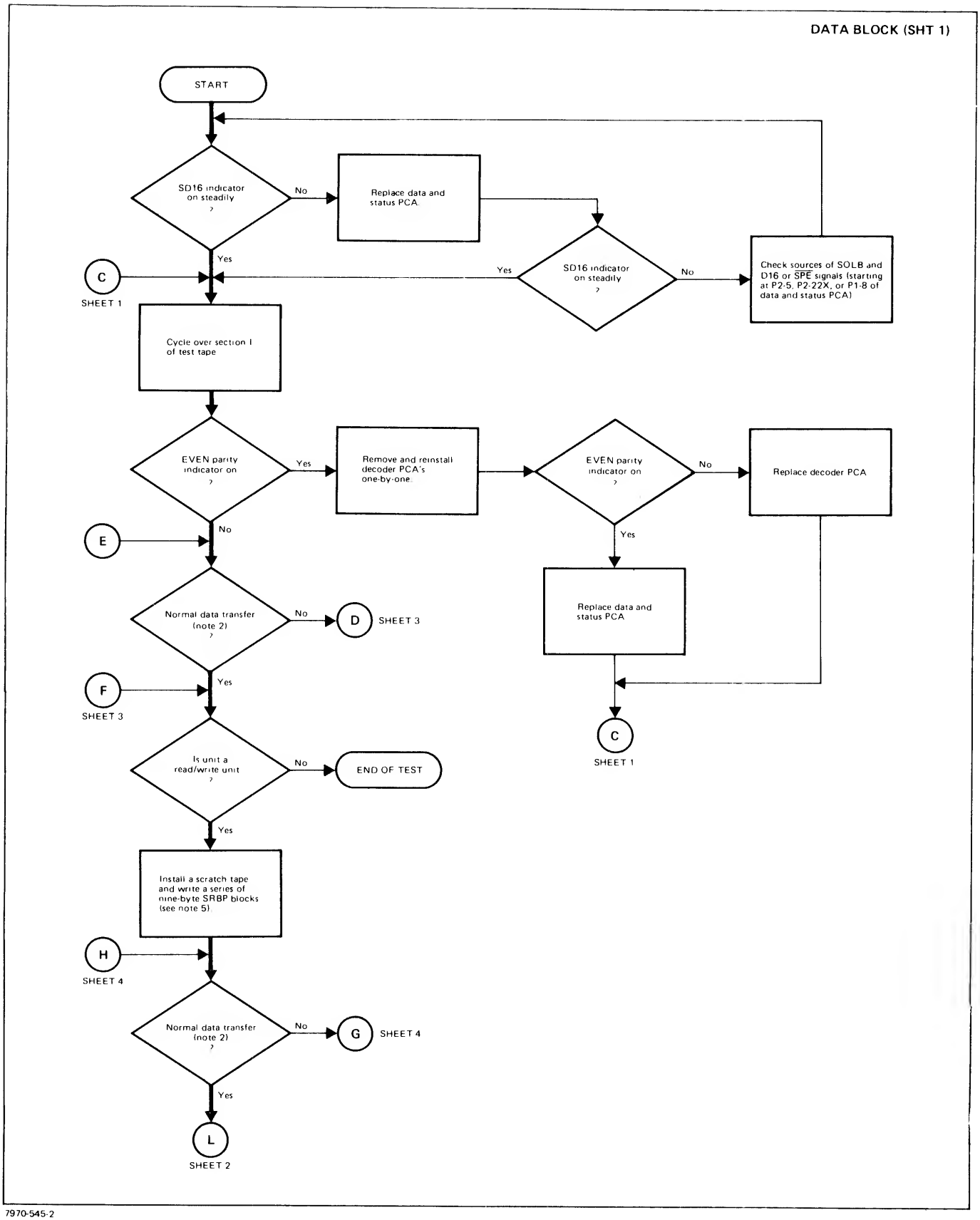
Horiz = 0.2 ms/cm
Vert = 2 V/cm

NOTES:

1. SRBP is an abbreviation for Single Rotating Bit Pattern.
2. The following listed conditions of the read data test PCA indicators indicate normal data transfer for a series of nine-byte SRBP blocks:
   a. EOB indicator lights momentarily after the end of each block.
   b. RC indicator lights once for each byte.
   c. Data indicators P and 0 through 6 dimly lighted and 7 brightly lighted.
   d. MTE, STE, and EVEN indicators off.
3. The following listed conditions of the read data test PCA indicate normal data transfer for a continuous SRBP block:
   a. EOB and EVEN indicators off.
   b. Data indicators P and 0 through 7 on.
   c. RC indicator lights once for each byte.
   d. STE and MTE indicators off initially (The STE indicator and then, sometime later, the MTE indicator might light occasionally throughout running of the same tape if the tape, tape heads, or tape path is dirty or defective).
4. The following listed conditions of the read data test PCA indicate normal data transfer for a series of preamble-no data-postamble blocks:
   a. EOB indicator lights at the end of each block.
   b. Data indicators P and 0 through 7, RC, EVEN, STE, and MTE indicators off.
5. Before performing the read-after-write portion of the test, ensure that the gap potentiometer on the write formatter test PCA is set for the proper between-blocks gap and that the 1600/3200 jumper is in position 4 (odd parity).
6. While running a continuous SRBP block in read-after-write mode, it is normal for a few STE's and MTE's to occur. This happens even when a new tape is used on a clean tape path. When they occur, cycle the END OF DATA switch on the write formatter test PCA.

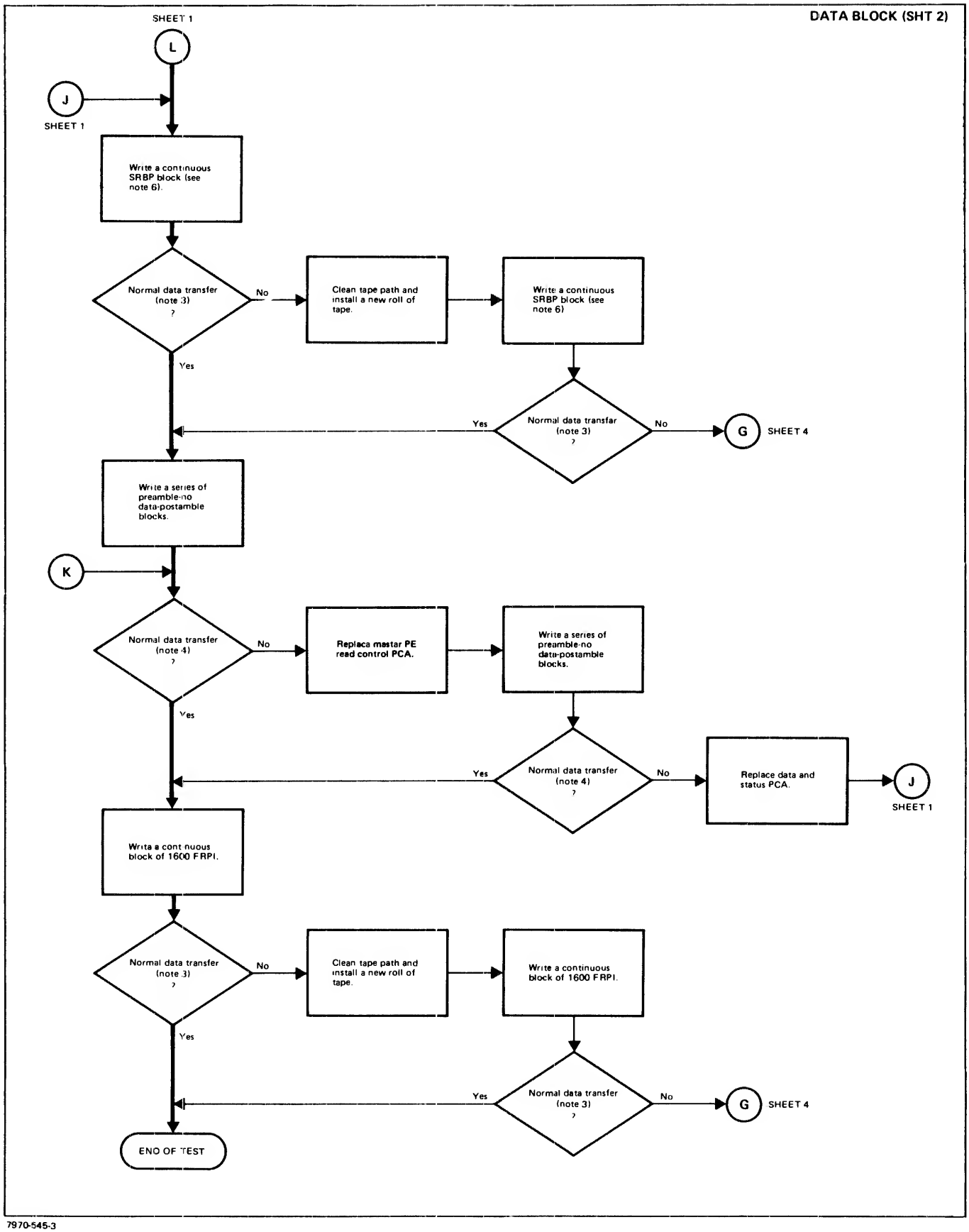
7970-545-1

Figure 5-12. Data Block Troubleshooting Flowchart (Sheet 1 of 5)



7970-545-2

Figure 5-12. Data Block Troubleshooting Flowchart
(Sheet 2 of 5)



7970-545-3

Figure 5-12. Data Block Troubleshooting Flowchart (Sheet 3 of 5)

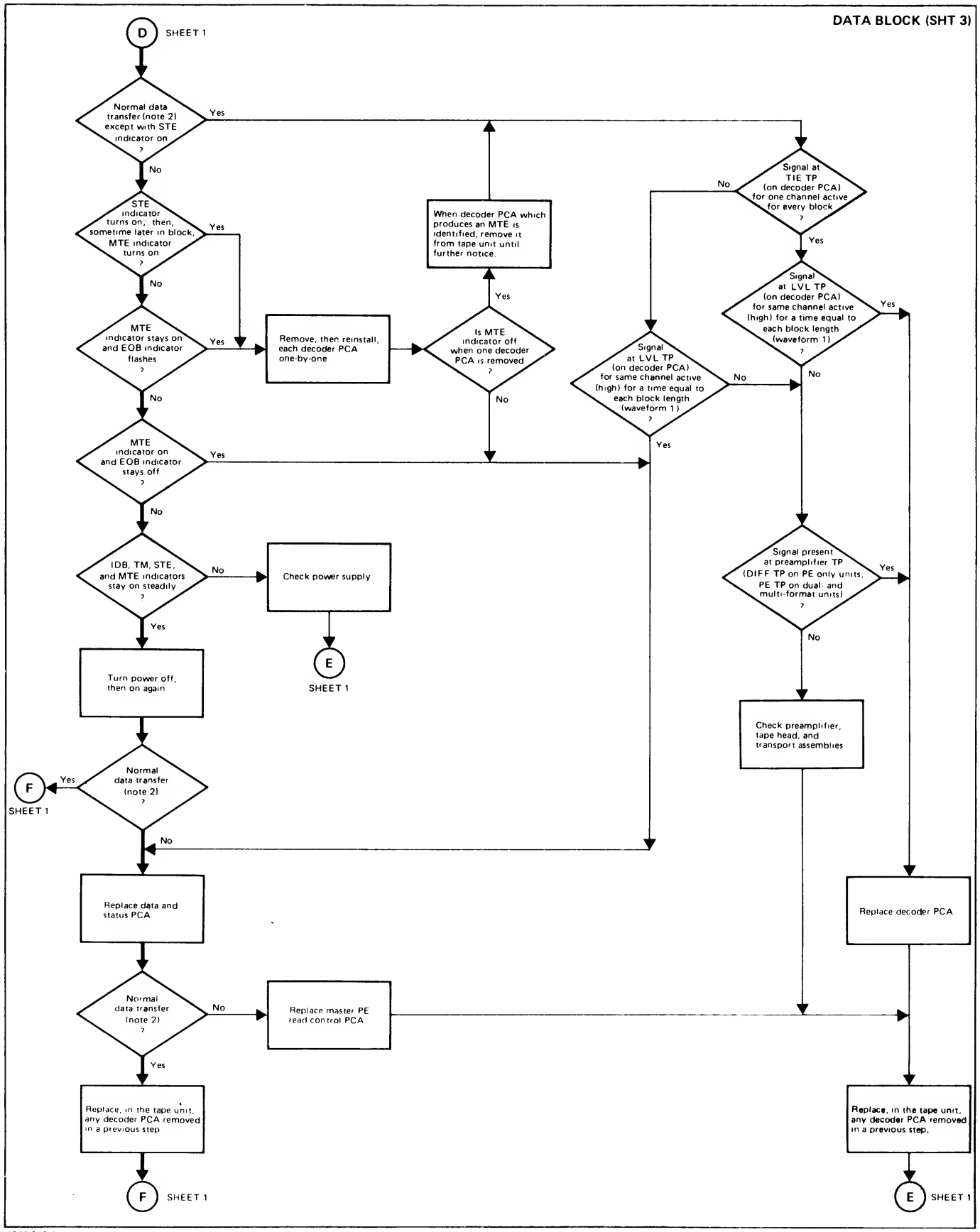
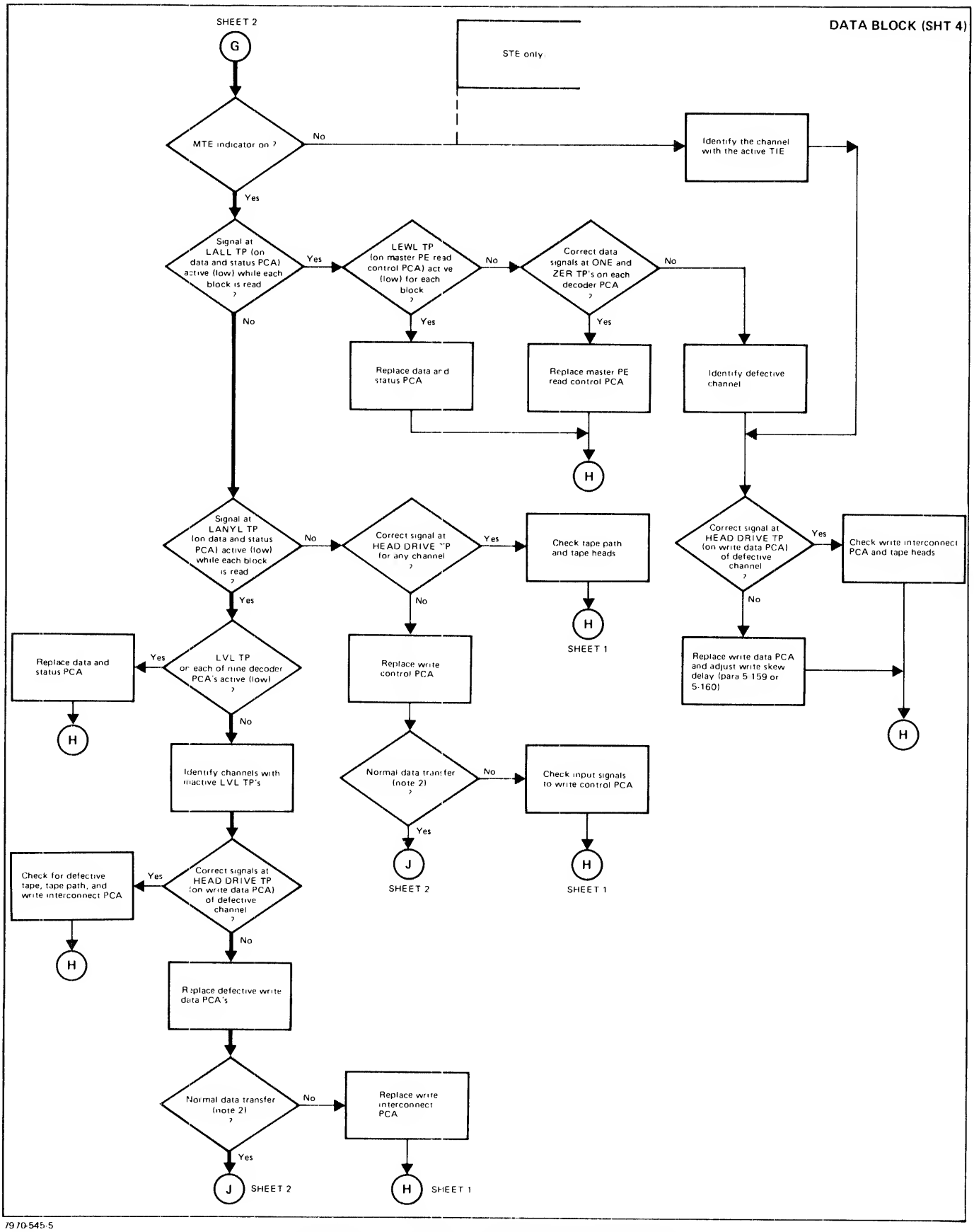


Figure 5-12. Data Block Troubleshooting Flowchart (Sheet 4 of 5)



7970-545-5

Figure 5-12. Data Block Troubleshooting Flowchart (Sheet 5 of 5)

Change 1
JULY 20, 1976

Manual Part No.: 07970-90887
Print Date: JUN 1976

CHANGE TO:

HP 7970B/E Digital Magnetic Tape Unit Service Manual

CHANGE DESCRIPTION: These changes to the manual are to reflect engineering changes and errata.

CHANGE INSTRUCTIONS:

1 Insert the enclosed numbered pages in the appropriate location in the manual and discard the old pages. (Except page 5-22).

2 Obsolete old page 5-22 and insert new pages 5-22, 5-22A, and 5-22B.

3 Errata changes as follows:

a. Page 1-9, remove art no's. from figure 1-4.

b. Page 4-26, paragraph 4-23 - any reference to sync generator should note series 1232 or older.

c. Page 5-43, in the CAUTION note first sentence is, "read full speed", should be "reach full speed".

d. Page 5-58, paragraph e, is "the parity jumper is set to the odd parity position." should be "the jumper near chip U32 is from 2 to 3."

e. Page 5-58, paragraph h., second sentence should read; The RC and EOB indicators should flash (appear as a bright light on higher speed models), the EVEN, STE, and MTE . . . . . Also in the second sentence "the P channel" should be "the number 7 channel".

f. Page 1-14, under OPERATING ENVIRONMENT Altitude IS 10,000 ft (3.048 m) S/B 10,000 ft (3.048 km)

g. Page 1-14, under HEAD GUIDE SPACING the word compatible is misspelled. S/B Compatible

HEWLETT PACKARD

SERVICE MANUAL

7970B/E

DIGITAL MAGNETIC TAPE UNITS

Manual Part No. 07970-90887
Microfiche Part No. 07970-90894

HEWLETT-PACKARD COMPANY
15 N. PHILLIPPI ST., BOISE, IDAHO, U.S.A.

PRINTED: JUN 1976
CHANGED: APR 1977

Title Page

SECTION IV. THEORY OF OPERATION (CONTINUED)

SECTION V. MAINTENANCE AND TROUBLESHOOTING

TABLE OF CONTENTS (CONTINUED)

Title Page

SECTION V. MAINTENANCE AND TROUBLESHOOTING (CONTINUED)

Title Page

SECTION V. MAINTENANCE AND TROUBLESHOOTING (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

Title Page

SECTION V. MAINTENANCE AND TROUBLESHOOTING (CONTINUED)

FIGURES

Figure Page

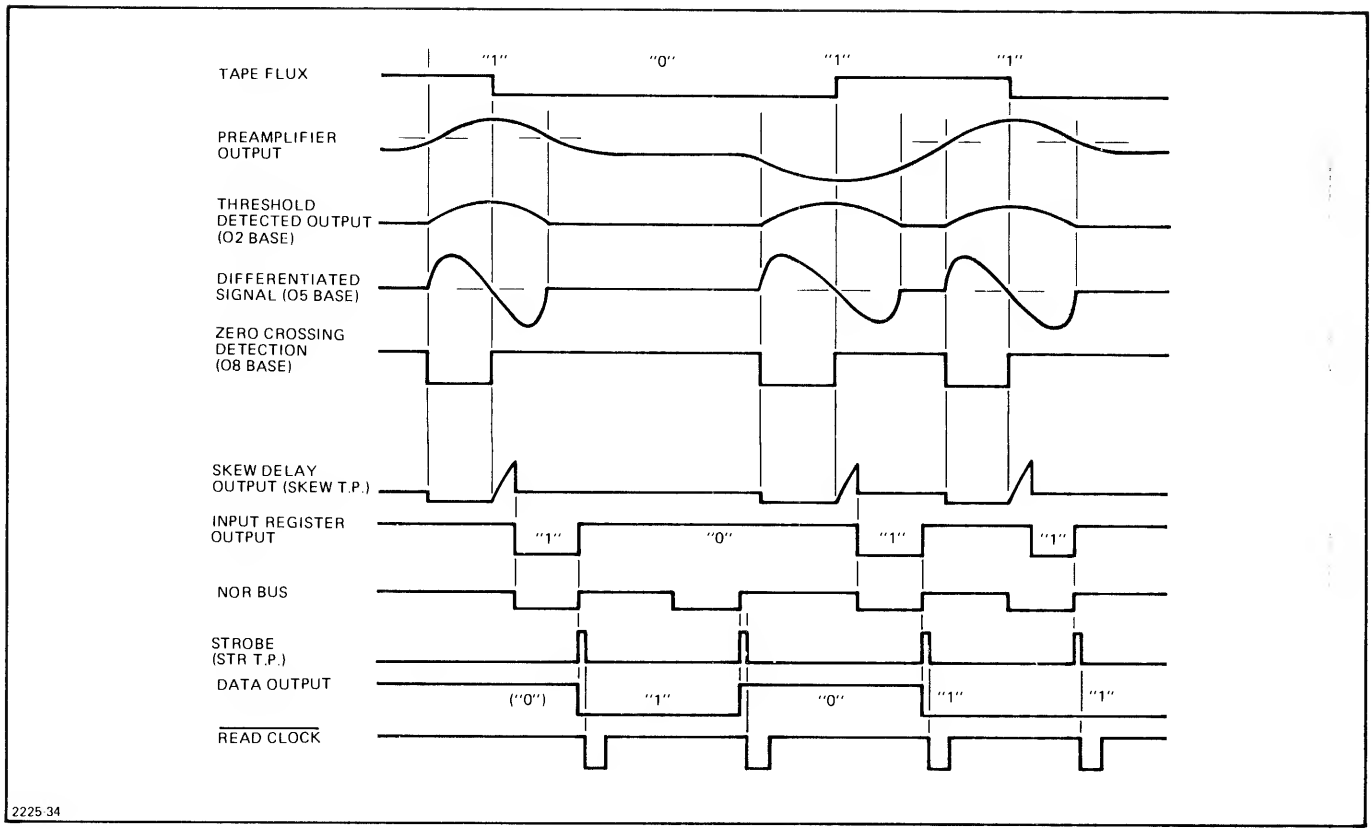


Figure 4-10. NRZI Circuits Waveforms

varied by adjusting the slope of the ramp. Skew adjustment is made by adjusting the ramp for each channel so that all ramp voltages terminate at the same time.

When a data "1" bit is processed through the input and delay circuits, the input register stores a "1" and activates the read "nor" bus. The "nor" bus receives signals form the input register of all nine channels. Therefore, it will be activated by the first channel which receives a "1". When the read "nor" bus is activated, the character gate generator on the read control PCA begins a voltage ramp which determines the length of the character gate. When the ramp reaches a threshold, the trigger circuit activates the Strobe one-shot multivibrator to generate the Read Strobe signal. The character gate begins when the read "nor" bus becomes active and ends when the Read Strobe signal becomes active. It is adjustable and is normally adjusted to be 45 percent of the nominal byte time. However, the byte time is different for different densities and tape speeds. Therefore, the character gate must be adjusted according to the tape speed and density of the tape data. The density select circuits indicate to the character gate generator the density selected on the multiple density select switch assembly. The character gate determines the length of time the "nor" bus is active.

When the Read Strobe signal is generated, a "1" or "0" is stored in the output register depending on whether or not a "1" is stored in the input register. Also, the input register is cleared at the same time. When the short duration Read Strobe signal ends, the Read Clock one-shot multivibrator generates the Read Clock signal which clocks the data bit present in the output register into the interface.

If a "0" occurs at the input of the read data PCA, the full wave rectifier, buffer, peak detector, high-gain amplifier, skew delay RC circuit, threshold generator, and input register will remain inactive. Since the input register has not stored a "1", when the Read Strobe occurs, a "0" will be stored in the output register and clocked out to the interface. The read control circuits operate as previously described to produce the Read Strobe because a "1" must occur on at least one of the nine channels for every byte.

4-19. PE Read Circuits Overall Functional Sequence Explanation.

The PE read circuits are state controlled. When the machine is in any given state it is given certain directions and makes certain decisions. The results of the decisions advances the machine to another operation or another state. State control logic sequences the activities of the data path circits during any PE Read operation. This data path consists of the Decoder, Data and Status, and the Read Control PCA's. The final decision is made when the proper conditions exist to generate output signals.

The PE read circuits operate in two modes; read only and read after write. Signals read off tape in read after write mode are required to meet more stringent requirements, before being recognized as valid than read only mode signals. This ensures reliability and compatability to industry standards.

Figure 4-11 is a flow diagram which is laid out and itemized to show the direct correlation of the state decisions to the logic shown on the schematics of the PCA's. (Refer to parts and diagrams manual). Each decision block within each state has a notation showing which PCA makes that decision, often the area on the PCA schematic is included.

4-20. PE Read Circuits State Control Sequence Discussion.

When power is applied to the PE read circuits, most sequencing and output circuits are reset, (State counter is reset at 0000). When a signal is detected in any of the nine channels, a check is made to determine if the PE read circuits are operating in read only or read after write mode. (State 00) refer to figure 4-11.

To show the use of the flow diagram in conjunction with the diagrams manual, let's say in the above decision we are in the Read after Write mode: The state counter advances from 00 to 04. (The state counter is discussed in the following information) once in state 04 (S04) the next decision is; do we have 5 consecutive byte times with a signal present on any channel? As shown on the flow diagram, this decision is made on the Read Control PCA and specifically in the state control logic. If we now refer to the read control PCA schematic, the output of U27C (NOR GATE)

is S04, count 5 (cnt 5), and signal present any channel (ANYL). (S04+CNT5+ANYL). If either CNT 5 or ANYL is a false or low signal, then this would correspond to a "NO" decision on the flow diagram. By NORING this output (false) at U44A with the term CNT36 we have two low signals on the input and a high on the output. The high output resets U111B (22FF) (through NAND gate U49A) and the state count goes from 4 (0100) to zero (0000).

Now look at U310A of the read control PCA. It's output is CNT5 and S04. This output goes to NAND GATE U38A and is gated with Identification signal (IDL). If this output is true the U111A (23FF) is set. This is a yes decision for the first two decisions on the flow diagram in state 04. Thus, the true output (U111A) causes the counter to go from S04 (0100) to S14 (1100), as indicated on the flow diagram.

The discussion above relates the method of using the flow diagram and the schematics for detailed circuit troubleshooting.

4-21. PE Read Circuits Overall Functional Discussion.

This discussion will reference to the previous state control logic explanation and the parts and diagrams manual. Also use paragraphs 4-2 and 4-3 as reference for general PE Code and tape information.

The following paragraphs trace signal flow from the tape heads to the interface. The discussion is based on the PE read circuits block diagram (figure 4-12). Paragraph 4-22 describes signal flow from the preamplifier to the level change register. Paragraph 4-23 traces the signal path from the threshold comparator to the amplitude detector, to produce the Level signal (the Level signal is required to enable other circuits), and through the sync generator and clock control circuits to the clock to produce the DF and 40 DF pulse trains. The DF and 40 DF pulse trains synchronize the PE read circuits. Paragraph 4-24 describes both operation of the circuits (amplitude detector, active channel logic, state control logic, and window generator) and the conditions required to activate and unlock the pointer register enable latch and enable the window logic, the pointer register enable latch must be unlocked to enable the skew buffer and the window logic must be enabled to produce the Shift signal which shifts data from the level change register into the skew buffer. Paragraph 4-25 provides a brief explanation of skew buffer operation. Then paragraph 4-26 describes operations of the error-correction register, parity checker, error correction circuits, and output register. Operation of the skew buffer output sensing circuits, end of data logic, state control logic, and output logic (which becomes significant during reading of the postamble) is described in paragraph 4-27. Paragraph 4-28 describes functions of the error detection circuits and the TIE decoder logic.

4-22. Signal Flow (Preamplifier to Level Change Register). The flow of signals through the PE read circuits (figure 4-12 and 4-13) is from the tape heads, through the preamplifier, differentiator and zero crossing detector. (These circuits might be located in either the master or slave tape unit, dependig on which is supplying the signals. If a slave unit is supplying the signals, the signals enter the master tape unit after being digitized by the zero crossing detector).

The signals are amplified by the preamplifier, the differentiator produces a crossing of the zero volts line for each tape flux reversal (peak), and the zero crossing detector digitizes the amplitude-varying signal from differentiator to produce logic 1's and 0's. If a slave tape unit is supplying the signals, they pass through the zero crossing enable logic to the level change register without restriction. However, if the master unit is providing the signals, the Master Read Enable (MREN) signal must be active to enable passage of the signals through the zero crossing enable logic. The MREN signal, which originates in the status logic on the data and status PCA, is active when the master tape unit is selected and on-line, the tape is moving and is past the beginning of tape (BOT) marker, and density 1600 is selected. The Read Enable signal generated by the control logic in the slave unit performs a function similar to the MREN signal in the master tape unit. The signals from zero crossing enable a logic one to be stored, momentarily, in the level change register as level changes (or level transitions). While in the level change register, the signals are applied, as the Level Transitions signal, to the skew buffer. However, the skew buffer can take no action until the pointer register enable latch and window logic are enabled.

4-23. Signal Flow (Threshold Comparator to Amplitude Detector, Sync Generator, and Clock). The output of the differentiator, in addition to being applied to the zero crossing detector, is also applied to the threshold comparator (in either the master or slave tape unit). The amplitude of the signal is compared, in the threshold comparator, with positive and negative thresholds generated by the threshold generator. (The thresholds are higher, requiring greater signal amplitude, in read-after-write mode). If the signal is of sufficient amplitude, to exceed the threshold, a digitized Amplitude Comparison (AC) signal is supplied by the comparision enable logic to the amplitude detector and sync generator. If the master tape unit is reading the tape, the MREN signal must be active for the comparison enable logic to pass the signal. This is not necessary if a slave unit is reading the tape. However, the same function is performed in the slave PE read circuits.

When the output of the differentiator is of insufficient amplitude to exceed the threshold level for three consecutive DF periods, the amplitude detector inhibits action of the window logic (the window logic must be enabled for data to pass through the decoder PCA) and notifies the error detection circuits in the channel logic, on the data and status PCA, that the channel with which it is associated has no threshold-exceeding input. The amplitude detector (for channel two only) also informs the clock control logic that channel two is receiving no threshold-exceeding input.

The channel two and channel P sync generators supply a Sync Pulse to the clock control circuits, for every level change (level transition) entering the level change register. This includes both transitions representing a logic 1 or logic 0 and phase correction transitions. The clock uses these pulses to determine the average length of time between bytes and adjusts the time of a Data Frequency period to this time. The clock, on the data and status PCA, generates two pulse trains; the data frequency (DF) pulse train and the 40 DF pulse train. Both are used to synchronize operation of the master PE read circuits. The 40 DF pulse train has a frequency 40 times greater than the DF pulse train. Thus, forty 40 DF pulses occur for each DF pulse. (The frequency of the 40 DF pulse train is also adjusted to agree with the average byte time).

5-34. FORWARD STATIC SKEW COMPENSATION ADJUSTMENTS. The techniques for rapid adjustment and for evaluating the need for adjustment differ. Figure 5-8 shows poor skew alignment and proper skew alignment. To adjust static skew compensation proceed as follows:

a. Load the Master Alignment Tape, HP part number 9162-0027, and place the tape unit in synchronous forward mode for the adjustment operation.

b. Adjust FWD skew delay control of channel 2 (Read data PCA) until resistor is approximately ¼ turn from the fully CCW position. Channel 2 will be reference channel for the remaining adjustments.

c. Connect the oscilloscope channel A probe to the SKEW test point of the reference channel (2). Connect the oscilloscope channel B probe to each SKEW test point in succession and algebraically add oscilloscope channels A and B.

d. Adjust the oscilloscope sweep to display at least one full bit time (leading edge of one bit to the leading edge of the next), with the oscilloscope vertical deflection at approximately 2V/cm.

e. Adjust each channel skew delay variable resistor for a maximum displayed amplitude and test waveform as shown in figure 5-8.

5-35. REVERSE STATIC SKEW COMPENSATION ADJUSTMENTS. Reverse static skew compensation is accomplished in exactly the same manner as that used for forward skew except for the use of reverse drive mode and adjustment of reverse skew controls. The same SKEW test points are used for both adjustments.

5-36. READ CHARACTER GATE ADJUSTMENTS. The read character gate is adjusted to allow a period equal to approximately 46 percent of the bit-to-bit distance for all of the read bits in a character to be placed in the output register.

a. Load the tape unit with the Master Alignment Tape, HP part number 9161-0027 (or any all "ones" 800 cpi tape), place the unit in synchronous forward operation, and select 800 cpi operation (multiple density units only).

b. Synchronize the oscilloscope (negative slope) to the NOR test point on the read control card. (The first data bit of a character will start the gate time when this line goes to ground).

c. Observe the bit-to-bit time (negative-going edge to negative-going edge). The low (or ground) portion of this signal represents the character gate time.

d. Using the gate control (R29) on the read control PCA, adjust the NOR (ground portion) of the signal to 46 percent of the nominal bit-to-bit time. Ensure that the bit-to-bit time is consistent with the data transfer rate (i.e. 50 micro-seconds for a 7970 operating at 25 IPS - 800CPI).

NOTE: Figure 5-9 can be used as a guide once the reader is familiar with the forgoing procedures.

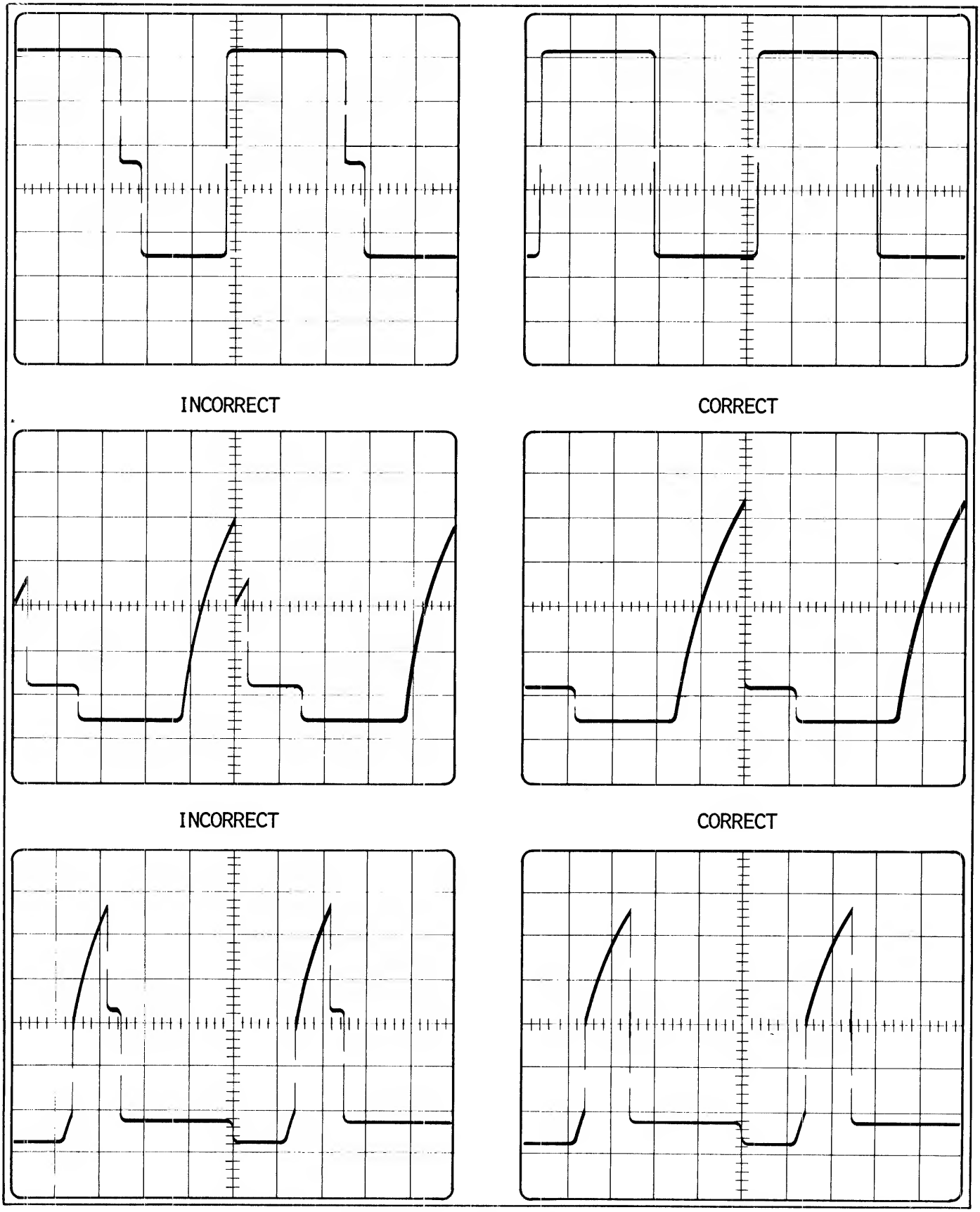


Figure 5-8. Skew Waveforms

5-37. WRITE ADJUSTMENT PROCEDURES, NRZI.

Load the tape transport with a reel of scratch tape equipped with a write enable ring. Place the unit in synchronous forward write mode and write a data pattern consisting of all "ones", at 800 cpi.

5-38. NEWLY UNPACKAGED UNITS. Newly unpackaged units, adjust the write skew delays as follows, all other units go to paragraph 5-39.

NOTE: Under no circumstances are any of the read skew adjustments to be changed during the write skew compensation process.

a. Adjust the channel 2 write skew delay until channel 2 variable resistor is approximately ¼ turn from the fully CCW position and connect the oscilloscope channel A probe to the read SKEW test point of this channel. Connect the oscilloscope channel B probe to the Read SKEW test point corresponding to the write data channel being adjusted (first time through, this is channel 2). Set the oscilloscope controls to algebraically add channels A and B. Adjust oscilloscope sweep to display at least one full bit time (leading edge of one bit to the leading edge of the next).

b. Adjust the skew delay variable resistor of the channel under adjustment to obtain a maximum amplitude on the oscilloscope display.

c. Set all channels to channel 2 by repeating steps a and b for all remaining channels except the reference channel (channel 2).

5-39. UNITS JUST REPAIRED OR IN USE. Do the following write skew adjustments.

Check all of the write channel skew adjustments and find the one most CCW.

a. Adjust this adjustment to the fully CCW position.

b. Compare and align channel 2 to this channel.

c. Set all channels to channel 2.

d. If one channel is still out of the specification set channel 2 to this one and repeat steps "c" and "d".

5-39A. WRITE ADJUSTMENT PROCEDURES, PE.

NOTE: Adjustment procedures for the write circuits consist of the skew delay for both master and slave units.

5-39B. WRITE SKEW DELAY ADJUSTMENT (MASTER UNITS). The write skew delay adjustments of master units are similar to the write skew delay adjustment of slave units except for test points monitored. Prior to performing the write skew adjustments, ensure that the read preamplifier adjustments are within tolerance. Skew delay is adjusted out of the PE write circuits by first determining the amount of

static skew delay in each channel of the PE read circuits. This is done by measuring the amount of skew, as compared to a reference channel, at the DAT test point of each PE read decoder PCA while reading a reference tape. Then the reference tape is removed, an unwritten tape is installed, and a read-after-write operation is performed. The write skew delay adjustment variable resistor (on the write data PCA's) for each channel is then adjusted to produce the same amount of skew delay (as compared to the reference channel) as was observed while reading the reference tape. This compensates for skew delay in the write circuits.

a. Install control and status test PCA, part number 13191-60010, write formatter, part number 13195-60000, and write formatter test PCA, part number 13196-60001 in the tape unit.

b. Load the tape unit with the master alignment tape, part number 9162-0027.

c. Monitor master unit decoder PC assembly DAT test points and place the unit in a read operation.

d. Observe the signal at the decoder test points and compare the time displacement of the positive-going edge of each channel. This time displacement is static skew. Note these displacements relative to a reference channel (preferably channel two). If these displacements are not within 300 microinches of the reference channel, head wear or amplifier failure are the probable causes. (To obtain static skew, in microinches, multiply the measured static skew, in microseconds, by the tape speed, in ips.)

e. Remove the alignment tape and load the tape unit with an unwritten reel of tape equipped with a write enable ring.

f. Place the unit in a write operation, writing a continuous 1600 frpi data pattern.

g. Measure the skew delay at the DAT test point of each decoder PCA. If all are within 50 microinches of the reference channel, ignore steps h through j.

h. Set all write skew delay variable resistors for minimum delay (fully counterclockwise).

i. Adjust channel two skew delay variable resistor clockwise to ensure that the trailing edge of channel two occurs slightly later than the trailing edge of the remaining channels. This step ensures a minimum setting of the write skew variable resistors.

j. Adjust each write skew delay variable resistor for the same amount of delay (compared to the reference channel) as was noted in step d.

5-39C. WRITE SKEW DELAY ADJUSTMENT (SLAVE UNIT). The write skew delay adjustment of slave units is similar to write skew delay adjustment of master units, except for test points monitored. Prior to performing the write skew adjustment, ensure that the read preamplifier adjustments are within tolerance.

a. Load the tape unit with master alignment tape, part number 9162-0027.

b. Install control and status test PCA, part number 13191-60010, write formatter, part number 13195-60000, and write formatter test PCA, part number 13196-60001 in the tape unit.

NOTE: Waveforms for a slave unit can be monitored at the DAT test points on the read decoder PCA's in the master unit, provided the slave unit is connected to the master unit and selected on the master unit select switch. If the slave unit is not connected to the master unit, monitor the waveforms at the test points on connector RSJ2 of the slave read PCA.

c. Monitor slave unit zero cross-over outputs using the 1.6k resistor adjacent to odd-numbered pins (beginning with 1X) as a test point.

d. Place the unit in a read operation and observe the zero cross-over signals. Note the time displacement of the negative-going edge of each channel relative to a reference channel (preferably channel two). This time displacement is static skew.

e. Remove the alignment tape and load the tape unit with an unwritten reel of tape equipped with a write enable ring.

f. Place the unit in a write operation, writing a continuous 1600 frpi data pattern.

g. Measure the skew delay at the DAT test point on the master unit decoder PCA for each channel. If all are within 50 microinches of the reference channel, ignore steps h through j.

h. Set all write skew delay variable resistors for minimum delay (fully counter-clockwise).

i. Adjust channel two skew delay variable resistor clockwise to ensure that the trailing edge of channel two occurs slightly later than the trailing edge of the remaining channels. This step ensures a minimum setting of the write skew variable resistors.

NOTE: The above step assures a minimum setting of the write skew variable resistors.

j. Refer to the static skew displacements noted during the read operation and adjust each write skew delay variable resistor to match the static skew displacements.

5-40. READ AND PERFORMANCE ADJUSTMENT PROCEDURES, PE.

The PE read circuits performance tests consist of an overall performance test, which checks all PE read circuit outputs, and other tests which check selected PE read circuits or functions. Also included is a description of PE read data test tape, part number 5080-4555. Knowledge of the contents of the test tape is required to know which circuits and functions are checked when a given portion of the tape is run. (Remove any grounds installed during a test at the end of that test.)

Change 2
SEP 1976

Manual Part No.: 07970-90887
Print Date: JUN 1976

CHANGE TO:

7970B/E Digital Magnetic Tape Units
Service Manual

CHANGE DESCRIPTION: These changes are to correct errors in the manual.

CHANGE INSTRUCTIONS:

1 Correct the error in the specification on page 5-18, paragraph 5-33 b. IS: 6.4V -0.5, +0.2V peak-to-peak.
S/B: 5.0V -0.5, +0.2V peak-to-peak.

2 Page 5-24, paragraph 5-51, NOTE: refers to paragraphs 5-62 and 5-63, S/B paragraphs 5-63 and 5-64.

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Europe: 1217 Meyrin-Geneva, Switzerland • Cable "HEWPACKSA" Tel. (022) 41.54.00

Change 3
JAN 1977

Manual Part No.: 07970-90887
Print Date: JUN 1976

CHANGE TO:

7970B/E Digital Magnetic Tape Units
Service Manual

CHANGE DESCRIPTION:

These changes are to correct errors and deletions in the manual.

CHANGE INSTRUCTIONS:

1

Remove pages supperceded and insert new pages supplied. The following pages are supplied:

v vi, 1-9 1-10, 1-11 1-12, 2-1 2-2, 3-7 3-8, 4-21 4-22, 4-25 4-26, 5-9 5-10, 5-11 5-12, 5-19 5-20, 5-31 5-32, 5-33 5-34, 5-39 5-40, 5-55 5-56, 5-57 5-58, 5-75 5-75A, 5-75B 5-76,

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Title Page

SECTION V. MAINTENANCE AND TROUBLESHOOTING (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

Title Page

SECTION V. MAINTENANCE AND TROUBLESHOOTING (CONTINUED)

FIGURES

Figure Page

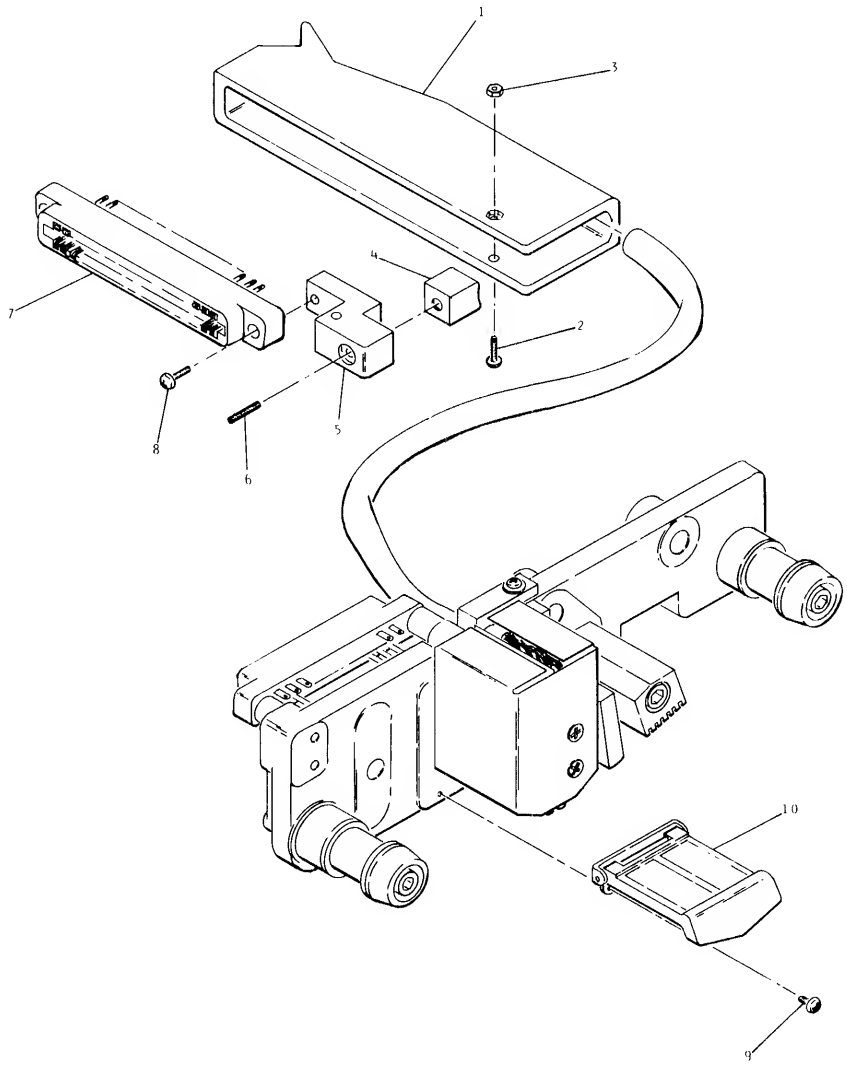


Figure 1-4. Magnetic Tape Head Assembly

facing the operator), the nine-track channel designations are 5, 7, 3, P, 2, 1, 0, 6, and 4. Seven-track channel designations from the reference edge are 7, 6, 5, 4, 3, 2, and P. The track channel designations are industry compatible.

1-18. READ ASSEMBLIES.

The read assemblies consist of a read preamplifier PCA, a card cage assembly (motherboard), a read control PCA, a single channel read data PCA, and three or four dual channel read data PCA's for seven-or nine-track operation, respectively. Refer to figures 1-2 and 1-3 for locations of these assemblies.

1-19. READ PREAMPLIFIER PCA.

The read preamplifier PCA contains nine identical amplifier circuits, one for each tape track. It amplifies the signals from the tape heads before they are applied to the read data and read control PCA's. Seven-track tape units have two unused channels (0, 1). The gain of each preamplifier is adjustable.

1-20. READ MOTHERBOARD ASSEMBLY.

The read motherboard assembly contains wiring for interconnecting the read preamp, read control and read data cards, and for interfacing with external circuits. 7970E slave units have a slave read assembly instead and the outputs go to the master unit read motherboard.

1-21. READ CONTROL PCA.

The read control PCA consists of circuits which control operation of the read data PCA's by establishing bias levels, providing voltage for read data skew delay circuits, and providing pulses used by the read data circuit to sample its output register.

1-22. READ DATA PCA'S.

The read data PCA's detect flux transitions in each track and produce a parallel digit output. This data is transferred to the output registers to provide the interface with a read data bit. Skew delay circuits compensate for nonperfect alignment of individual track gaps in the read head (gap scatter).

1-23. DECODER PCA.

(7970E). The decoder PCA's decode the PE data (separate data from phase correction signals and noise). The track error detection takes place here also.

1-24. DATA AND STATUS PCA.

The data and status PCA uses sync pulses developed from the data flow to generate a clock DF (DF = data frequency) and 40DF signal, these signals are used for timing throughout data flow. It also gives data status (i.e., do we have data?, do we have parity?) and contains the threshold generator.

1-25. WRITE ASSEMBLIES.

The write assemblies consist of a write interconnect assembly, card cage assembly (motherboard), a write control PCA, a single channel write data PCA, and three or four dual channel write data PCA's for seven- or nine-track operation respectively. Refer to figures 1-2 and 1-3 for location of these assemblies.

1-26. WRITE MOTHERBOARD ASSEMBLY.

The write motherboard assembly contains wiring for connecting the write control PCA and the write data PCA's to the write head. It also interfaces the write circuits with external circuits.

1-27. WRITE INTERCONNECT PCA.

The write interconnect PCA contains load resistors for all write drivers. It interconnects the head assembly with the write assembly and is located near the head assembly.

1-28. WRITE CONTROL PCA.

The write control PCA processes tape unit motion status signals and interface commands to control the write data circuits. When unit write condition is first established, the write control circuits ensure that the write head drivers are in a reset state (inter-record gap flux) and tape is saturated in the same polarity as the erase head.

1-29. WRITE DATA PCA'S.

The write data PCA's contain skew delay circuits to compensate for write head gap scatter and write head drivers which saturate the write heads for flux reversals.

1-30. POWER DISTRIBUTION ASSEMBLY.

The power distribution assembly consists of a transformer assembly, a power distribution PCA, and a power regulator PCA. The bottom section of the tape unit housing rear panel may be removed to gain access to the power supply components. Refer to figure 1-3 for locations of these assemblies.

1-31. TRANSFORMER ASSEMBLY.

The transformer assembly consists of a metal panel upon which are mounted the primary fuses, the 115V/230V switch for power source selection, a filter, the transformer, and three bridge rectifier circuits.

1-32. POWER DISTRIBUTION PCA.

The power distribution PCA contains the secondary fuses, filter capacitors and resistors, diodes, and three series regulator power transistors mounted on a heat sink. (5 power transistors on 7970E Master Tape Drives).

1-33. POWER REGULATOR PCA.

The power regulator PCA contains components for three regulator circuits which control current through the +12 volt, -12 volt, and -5 volt series regulator transistors. It also contains circuits for supplying additional power to the reel servo circuits under conditions of high speed forward and reverse tape movement.

1-34. SPECIFICATIONS.

Specifications of the tape unit equipped with read and write modules and all available options are listed in table 1-3.

1-35. ACCESSORIES FURNISHED.

The following accessories are furnishable with the standard tape unit.

Part No.	Description	Qty.
07970-00580	Rack Mounting Bracket	1
2190-0034	Lockwasher, no. 10	7
2680-0103	Screw, no. 10-32, 0.5 inch	7
2680-0116	Screw, no. 10-32, 0.375 inch.	4
3050-0002	Washer, Flat	7
8120-1348	AC Power Cable	1
1490-0738	Magnetic Tape Reel	1

1-36. ACCESSORIES AVAILABLE.

The following accessories are available for the tape unit at extra cost.

a. HP 13190A Multiunit Cable (12.5 feet).

b. HP 13190B Multiunit Cable (20 feet).

c. Transport Test Tape, part number 5080-4525 (for seven track application).

INSTALLATION

SECTION II

2-1. INTRODUCTION.

This section contains installation information and information pertaining to unpacking, inspection, claims for damage, site selection, and reshipping procedures.

2-2. SITE SELECTION.

The tape unit is designed for operation at sites that are not subject to excessive shocks, excessive vibration, or wide ranges of ambient temperatures. The unit should be located to provide access to both front and rear sections of the cabinet with sufficient room for the maximum swing radius of the cover door and the main casting door. Convection cooling is provided by perforated top, bottom, and rear lower panels. No forced air ventilation is required where the exterior ambient temperature does not exceed 131^{O}F and no other heat generating equipment is housed in the cabinet.

2-3. UNPACKING AND INSPECTION.

If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the unit is unpacked. Inspect the unit for damage (cracks, broken parts, etc.). If the unit is damaged and fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual). Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged unit without waiting for any claims against the carrier to be settled.

When unpacking the unit, retain all packing materials and hardware for future use. The following procedures describe how to unpack the unit in order to save all packing materials.

a. Using a sharp knife or similar tool, cut the top seal of the outer shipping box.

b. Remove the six toro pads isolating the inner shipping box.

c. Cut the top seal of the inner shipping box and remove accessory cartons or filler cartons.

d. Remove accessory liner and top pad.

e. Remove plastic sheet from face of unit.

CAUTION

The unit weighs up to approximately 140 pounds (63.56 kg). Two persons are required to lift the unit from the shipping container.

f. Remove unit from inner shipping box.

g. Remove the two number 10-32 screws and washers that secure the right-hand side of tape unit door casting to the housing.

2-4. INSTALLATION.

Installation of the tape unit is limited to mounting the unit in a standard 19-inch rack and connecting interface cabling. The following procedures describe the installation of the unit in a 19-inch rack.

CAUTION

The weight of the transport in the open position must be considered and ballast may be required to prevent the rack from tipping forward.

a. Remove protective covering from accessory kit and locate four number 10-32 flat head screws (part number 2680-0116) and rack mounting bracket (part number 07970-00580).

b. Attach the rack mounting bracket to the left rail of the rack with the four number 10-32 flat head screws. Orient the rack mounting bracket so that the upper and lower flanges face the inside of the rack. These flanges form a cradle to hold the left (hinged) side of the tape unit.

c. Place the tape unit into position and using three number 10-32, 0.5-inch machine screws (part number 2680-0103), three flat washers, and three lockwashers, attach the right side of the transport housing to the 19-inch rack.

d. Using the remaining four number 10-32, 0.5-inch machine screws (part number 2680-0103), flat washers and lockwashers, secure the left side of the transport housing to the rack mounting bracket.

WARNING

The tape unit power cable is equipped with a three-wire connector. Do not defeat the ground connection by using an adapter or breaking the grounding pin of the connector. Isolating the unit from ground creates a hazardous condition which may result in death or serious injury.

e. Connect the female polarized connector of power cable W1 to the male power connector of the tape unit. Route the power cable to the site power outlet.

l. Press ON-LINE pushbutton and release.

(1) ON-LINE pushbutton indicator will illuminate.

(2) The tape unit is now ready for processor control.

(3) The on-line condition negates the REWIND and LOAD pushbutton circuits.

(4) Press REWIND pushbutton; press LOAD pushbutton and observe transport response. No response should be observed.

(5) To remove the unit from on-line status, press RESET pushbutton.

(6) A substantial number of logic functions are initiated by the ON-LINE pushbutton. However, the following logic functions must occur before the unit is gated to status ready.

a. The On-Line signal is "and" gated with a Load Complete signal to generate a Ready signal.

b. The Ready signal is "and" gated with a Select-On-Line-Address (SOLA) signal to generate a Ready Status (SR) signal for the processor. (SR indicates that tape unit is selected, is on-line the initial loading sequence is complete, and the tape is not reqinding).

m. Press RESET pushbutton.

(1) ON-LINE indicator will go dark and RESET pushbutton will illuminate.

(2) Unit is now in off-line status. Manual controls are operative.

n. Check REWIND and capstan manual controls as follows:

(1) Open cover door and release transport main casting latch.

(2) Close cover door.

(3) Swing main casting door open.

(4) Set capstan servo FWD switch to ON (up). Observe that tape moves in forward direction.

(5) Set FWD switch to OFF. Observe that tape motion stops.

(6) Set capstan servo +160 (ips) switch to ON.

a. Observe that tape winds onto takeup reel at high speed.

b. Allow approximately 100 feet of tape to wind on takeup reel (seven or eight seconds).

c. Set +160 switch to OFF. Observe that tape motion stops.

(7) Set capstan servo REV switch to ON.

a. Observe that tape moves in reverse direction.

b. Set REV switch to OFF. Observe that tape movement stops.

(8) Press REWIND pushbutton (control panel). Observe that tape winds onto supply reel at high speed.

(9) Press RESET pushbutton.

a. Observe that tape movement stops.

b. REWIND pushbutton will go off.

c. RESET indicator will illuminate.

(10) Press REWIND pushbutton.

a. Observe that transport goes into fast rewind.

b. Close cover door.

c. Observe that RESET indicator is on.

d. Observe that REWIND indicator is illuminated.

e. Observe that tape winds past the loadpoint tab, stops, searches for the loadpoint, and comes to stop at loadpoint.

f. Observe that LOAD indicator illuminates.

(11) Hold REWIND pushbutton down until BOT tab passes photosense unit and then release pushbutton.

a. Observe that tape winds off the takeup reel.

b. Observe that REWIND pushbutton goes dark.

c. The following pushbutton indicators will illuminate: RESET, DENSITY SELECT, and ADDRESS SELECT.

o. Remove supply reel and install write enable ring.

p. Install supply reel. Observe that WRITE ENABLE indicator is illuminated.

q. Return unit to original configuration.

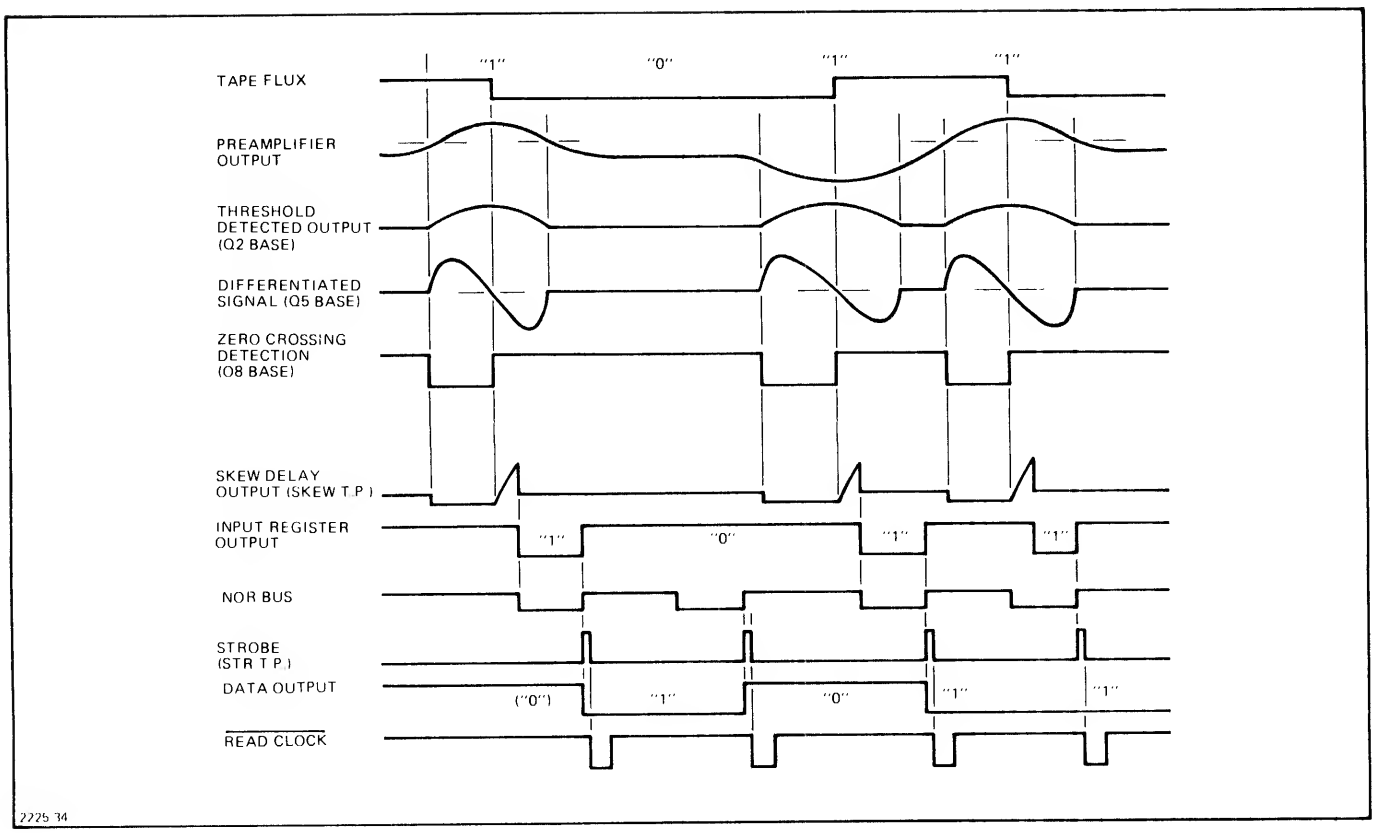


Figure 4-10. NRZI Circuits Waveforms

varied by adjusting the slope of the ramp. Skew adjustment is made by adjusting the ramp for each channel so that all ramp voltages terminate at the same time.

When a data "1" bit is processed through the input and delay circuits, the input register stores a "1" and activates the read "nor" bus. The "nor" bus receives signals from the input register of all nine channels. Therefore, it will be activated by the first channel which receives a "1". When the read "nor" bus is activated, the character gate generator on the read control PCA begins a voltage ramp which determines the length of the character gate. When the ramp reaches a threshold, the trigger circuit activates the Strobe one-shot multivibrator to generate the Read Strobe signal. The character gate begins when the read "nor" bus becomes active and ends when the Read Strobe signal becomes active. It is adjustable and is normally adjusted to be 45 percent of the nominal byte time. However, the byte time is different for different densities and tape speeds. Therefore, the character gate must be adjusted according to the tape speed and density of the tape data. The density select circuits indicate to the character gate generator the density selected on the multiple density select switch assembly. The character gate determines the length of time the "nor" bus is active.

When the Read Strobe signal is generated, a "1" or "0" is stored in the output register depending on whether or not a "1" is stored in the input register. Also, the input register is cleared at the same time. When the short duration Read Strobe signal ends, the Read Clock one-shot multivibrator generates the Read Clock signal which clocks the data bit present in the output register into the interface.

If a "0" occurs at the input of the read data PCA, the full wave rectifier, buffer, peak detector, high-gain amplifier, skew delay RC circuit, threshold generator, and input register will remain inactive. Since the input register has not stored a "1", when the Read Strobe occurs, a "0" will be stored in the output register and clocked out to the interface. The read control circuits operate as previously described to produce the Read Strobe because a "1" must occur on at least one of the nine channels for every byte.

4-19. PE Read Circuits Overall Functional Sequence Explanation.

The PE read circuits are state controlled. When the machine is in any given state it is given certain directions and makes certain decisions. The results of the decisions advances the machine to another operation or another state. State control logic sequences the activities of the data path circuits during any PE Read operation. This data path consists of the Decoder, Data and Status, and the Read Control PCA's. The final decision is made when the proper conditions exist to generate output signals.

The PE read circuits operate in two modes; read only and read after write. Signals read off tape in read after write mode are required to meet more stringent requirements, before being recognized as valid than read only mode signals. This ensures reliability and compatability to industry standards.

Figure 4-11 is a flow diagram which is laid out and itemized to show the direct correlation of the state decisions to the logic shown on the schematics of the PCA's. (Refer to parts and diagrams manual). Each decision block within each state has a notation showing which PCA makes that decision, often the area on the PCA schematic is included.

4-20. PE Read Circuits State Control Sequence Discussion.

When power is applied to the PE read circuits, most sequencing and output circuits are reset, (State counter is reset at 0000). When a signal is detected in any of the nine channels, a check is made to determine if the PE read circuits are operating in read only or read after write mode. (State 00) refer to figure 4-11.

To show the use of the flow diagram in conjunction with the diagrams manual, let's say in the above decision we are in the Read after Write mode: The state counter advances from 00 to 04. (The state counter is discussed in the following information) once in state 04 (S04) the next decision is; do we have 5 consecutive byte times with a signal present on any channel? As shown on the flow diagram, this decision is made on the Read Control PCA and specifically in the state control logic. If we now refer to the read control PCA schematic, the output of U27C (NOR GATE)

is S04, count 5 (cnt 5), and signal present any channel (ANYL). $\overline{(\overline{S04}+CNT5+ANYL)}$. If either CNT 5 or ANYL is a false or low signal, then this would correspond to a "NO" decision on the flow diagram. By NORING this output (false) at U44A with the term CNT36 we have two low signals on the input and a high on the output. The high output resets U111B (22FF) (through NAND gate U49A) and the state count goes from 4 (0100) to zero (0000).

Now look at U310A of the read control PCA. It's output is CNT5 and S04. This output goes to NAND GATE U38A and is gated with Identification signal (IDL). If this output is true the U111A (23FF) is set. This is a yes decision for the first two decisions on the flow diagram in state 04. Thus, the true output (U111A) causes the counter to go from S04 (0100) to S14 (1100), as indicated on the flow diagram.

The discussion above relates the method of using the flow diagram and the schematics for detailed circuit troubleshooting.

4-21. PE Read Circuits Overall Functional Discussion.

This discussion will reference to the previous state control logic explanation and the parts and diagrams manual. Also use paragraphs 4-2 and 4-3 as reference for general PE Code and tape information.

The following paragraphs trace signal flow from the tape heads to the interface. The discussion is based on the PE read circuits block diagram (figure 4-12). Paragraph 4-22 describes signal flow from the preamplifier to the level change register. Paragraph 4-23 traces the signal path from the threshold comparator to the amplitude detector, to produce the Level signal (the Level signal is required to enable other circuits), and through the sync generator and clock control circuits to the clock to produce the DF and 40 DF pulse trains. The DF and 40 DF pulse trains synchronize the PE read circuits. Paragraph 4-24 describes both operation of the circuits (amplitude detector, active channel logic, state control logic, and window generator) and the conditions required to activate and unlock the pointer register enable latch and enable the window logic, the pointer register enable latch must be unlocked to enable the skew buffer and the window logic must be enabled to produce the Shift signal which shifts data from the level change register into the skew buffer. Paragraph 4-25 provides a brief explanation of skew buffer operation. Then paragraph 4-26 describes operations of the error-correction register, parity checker, error correction circuits, and output register. Operation of the skew buffer output sensing circuits, end of data logic, state control logic, and output logic (which becomes significant during reading of the postamble) is described in paragraph 4-27. Paragraph 4-28 describes functions of the error detection circuits and the TIE decoder logic.

4-22. Signal Flow (Preamplifier to Level Change Register). The flow of signals through the PE read circuits (figure 4-12 and 4-13) is from the tape heads, through the preamplifier, differentiator and zero crossing detector. (These circuits might be located in either the master or slave tape unit, dependig on which is supplying the signals. If a slave unit is supplying the signals, the signals enter the master tape unit after being digitized by the zero crossing detector).

The signals are amplified by the preamplifier, the differentiator produces a crossing of the zero volts line for each tape flux reversal (peak), and the zero crossing detector digitizes the amplitude-varying signal from differentiator to produce logic 1's and 0's. If a slave tape unit is supplying the signals, they pass through the zero crossing enable logic to the level change register without restriction. However, if the master unit is providing the signals, the Master Read Enable (MREN) signal must be active to enable passage of the signals through the zero crossing enable logic. The MREN signal, which originates in the status logic on the data and status PCA, is active when the master tape unit is selected and on-line, the tape is moving and is past the beginning of tape (BOT) marker, and density 1600 is selected. The Read Enable signal generated by the control logic in the slave unit performs a function similar to the MREN signal in the master tape unit. The signals from zero crossing enable a logic one to be stored, momentarily, in the level change register as level changes (or level transitions). While in the level change register, the signals are applied, as the Level Transitions signal, to the skew buffer. However, the skew buffer can take no action until the pointer register enable latch and window logic are enabled.

4-23. Signal Flow (Threshold Comparator to Amplitude Detector, Sync Generator, and Clock). The output of the differentiator, in addition to being applied to the zero crossing detector, is also applied to the threshold comparator (in either the master or slave tape unit). The amplitude of the signal is compared, in the threshold comparator, with positive and negative thresholds generated by the threshold generator. (The thresholds are higher, requiring greater signal amplitude, in read-after-write mode). If the signal is of sufficient amplitude, to exceed the threshold, a digitized Amplitude Comparison (AC) signal is supplied by the comparision enable logic to the amplitude detector and sync generator (if present). If the master tape unit is reading the tape, the MREN signal must be active for the comparison enable logic to pass the signal. This is not necessary if a slave unit is reading the tape. However, the same function is performed in the slave PE read circuits.

When the output of the differentiator is of insufficient amplitude to exceed the threshold level for three consecutive DF periods, the amplitude detector inhibits action of the window logic (the window logic must be enabled for data to pass through the decoder PCA) and notifies the error detection circuits in the channel logic, on the data and status PCA, that the channel with which it is associated has no threshold-exceeding input. The amplitude detector (for channel two only) also informs the clock control logic that channel two is receiving no threshold-exceeding input.

The channel two and channel P sync generators supply a Sync Pulse to the clock control circuits, for every level change (level transition) entering the level change register. This includes both transitions representing a logic 1 or logic 0 and phase correction transitions. The clock uses these pulses to determine the average length of time between bytes and adjusts the time of a Data Frequency period to this time. The clock, on the data and status PCA, generates two pulse trains; the data frequency (DF) pulse train and the 40 DF pulse train. Both are used to synchronize operation of the master PE read circuits. The 40 DF pulse train has a frequency 40 times greater than the DF pulse train. Thus, forty 40 DF pulses occur for each DF pulse. (The frequency of the 40 DF pulse train is also adjusted to agree with the average byte time).

1) Loosen write enable assembly mounting screws.

2) Position the write enable assembly So that the sensing finger will clear the reel flange diameter throughout solenoid travel.

3) Tighten write enable assembly mounting screws.

5-20. REEL RETAINING KNOB. This adjustment is made during manufacture but may require some correction during the life of the tape unit. When the locking lever is working properly, it should be possible to place the reel over the rubber with a minimum of interference. When the locking lever is closed, positive resistance should be encountered as the rubber is compressed. In the locked position, it should not be possible to move the reel, (with respect to the hub) by hand. If slippage is suspected, place a piece of masking tape on the reel, another on the hub. A mark placed in alignment on both pieces of tape should not become misaligned by more than 1/8 inch in 16 hours of operation. To correct tape reel slippage, release locking lever and loosen the pozidrive screw, rotate the reel retainer knob clockwise, and tighten screw. Repeat until tape reel mounts firmly and does not slip. The tip of the screw fits into notches of the turntable. If the screw does not seat all the way down, back off and move the hub on the turntable a slight amount and retighten screw.

5-21. ELECTRICAL ADJUSTMENTS.

The electrical adjustments of the tape unit are very critical and must be performed in the following sequence.

a. Power supply adjustments.

b. Capstan motor offset current adjustment.

c. Capstan servo forward and reverse drive speed adjustments.

d. Capstan servo high-speed forward adjustment.

e. Capstan servo high-speed reverse adjustment.

f. Capstan servo ramp slope adjustment.

g. Reel servo adjustments.

5-22. POWER SUPPLY ADJUSTMENTS. Only one adjustment is provided for the three regulated supplies. The adjustment control is located in the circuitry for the +12-volt supply but is adjusted to establish the value of the +5-volt supply, which is held to a tighter operating tolerance. The value of the +12 and -12 volt supplies is established by a precision resistor network. The adjustment control, +5V, +12V, and -12V test points are located on the power regulator printed circuit assembly. Voltage is correctly adjusted when the following conditions are met:

a. +5 ± 0.050 Vdc. (Adjust to + 0.010 Vdc when adjustment is required).

b. +12 ± 0.360 Vdc.

c. -12 ± 0.360 Vdc.

NOTE: Final reel servo adjustments must be made after the capstan servo adjustments. The capstan speed must be within tolerance in order to properly adjust the reel servo adjustments. If the tape unit does not maintain tension, perform the reel servo adjustments initially, complete the capstan servo adjustments, and repeat the reel servo adjustments.

5-23. CAPSTAN MOTOR OFFSET CURRENT ADJUSTMENT. Prior to making the capstan motor offset current adjustment, verify that the power supply voltages have been adjusted.

For capstan switch and adjustment locations see figure 5-3.

Connect a suitable dc voltmeter (capable of resolution to ±5 mv dc) across the 3-ohm resistor (R21 or R22) connected in series with the capstan motor. The common side of the resistance is associated with pin 2 of CJ1 and the high or motor side is associated with pin 2 of CJ2.

Load the tape transport and be sure the tape is stopped. Adjust OFFSET control until voltmeter reading is minimum. Typical adjustment at room ambient temperature (25 C) will be in the order of ± 0.100 Vdc.

5-24. CAPSTAN SERVO FORWARD AND REVERSE DRIVE SPEED ADJUSTMENTS. Prior to performing the servo forward and reverse drive speed adjustment, ensure that power supply voltages and offset current are within tolerance. Figure 5-3 shows the location of service switches and forward and reverse speed adjustments used in the next step.

Accurate adjustment is based on reading (into a counter) data bits that have been recorded with high average accuracy. The 5080-4525 and 5081-9401 Test Tapes have bit-to-bit accuracy of better than 0.1 percent when measured over 2000 bits or more. In using this tape, it is important to recognize that there are two data bits for each cycle counted when the counter is connected to the preamplifier analog output signal. Also the frequency at other than the specified tape speeds may be calculated on a direct ratio basis.

a. Load test tape (5080-4525 and 5081-9401) and place unit in forward drive mode using FWD service switch (S2).

b. The test tape provides a signal of 10,000 Hz at a tape speed of 30 ips and has a bit-to-bit distance of 0.0015 inch.

c. The signal used for the following adjustments appears in preamplifier channel 3 of nine-track units and preamplifier channel 6 of seven-track units.

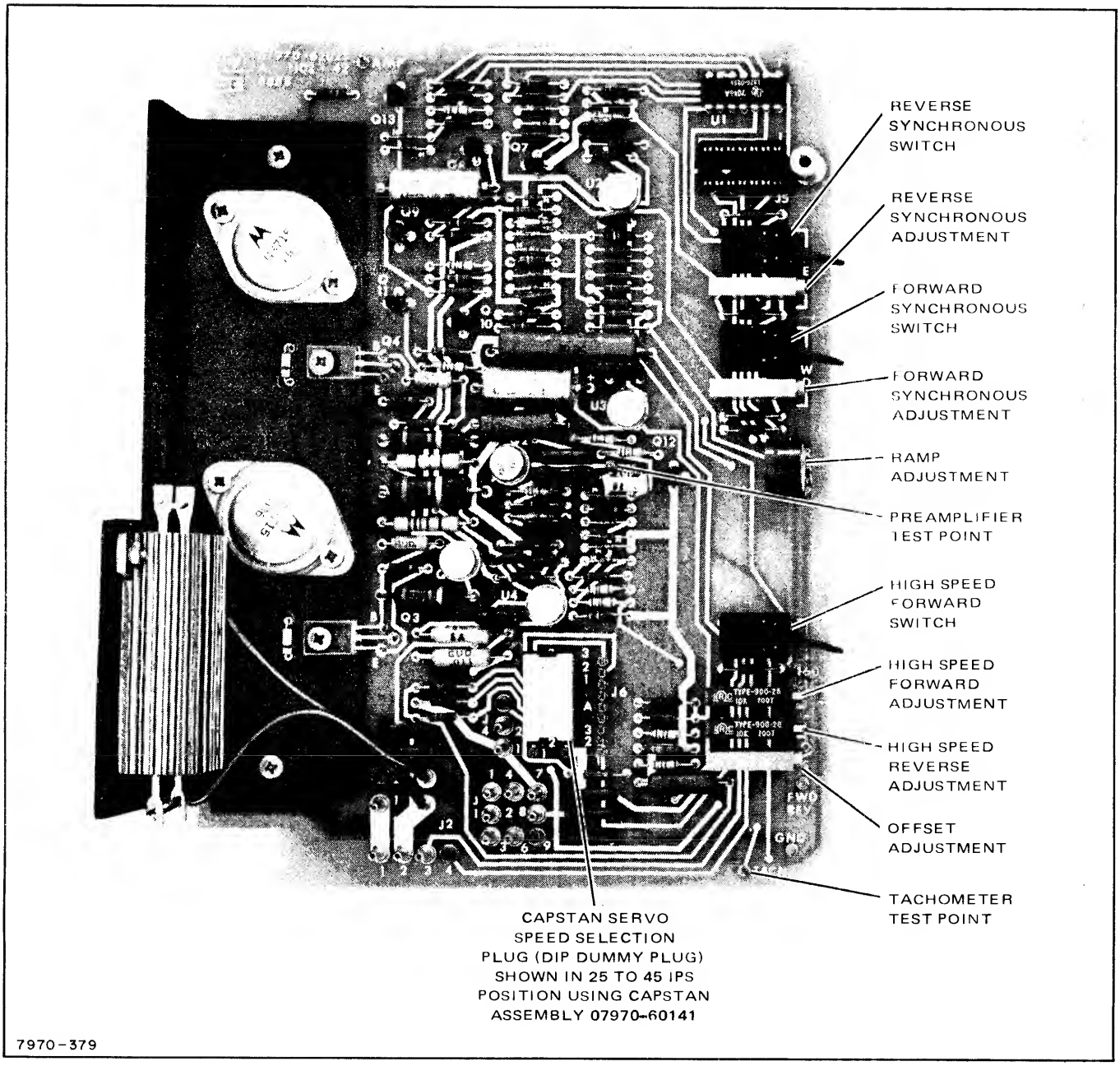


Figure 5-3. Single Speed Capstan Servo PC Assembly, Test Points and Adjustments

d. Adjust the FWD synchronous control (R34) if necessary, until counter indication is as follows:

(1) For 25 ips speeds, the counter indication should be 8,333 ± 83 Hz. If adjustment is necessary, adjust to 8,333 ± 16 Hz.

(2) For 37.5 ips speed units, the counter indication should be 12,500 ± 125 Hz. If adjustment is necessary, adjust to 12,500 ± 25 Hz.

(3) For 45 ips speed units, the counter indication should be 15,000 ± 150 Hz. If adjustment is necessary, adjust to 15,000 ± 30 Hz.

e. Repeat steps "a", "b", "c", and "d" with unit in reverse drive mode.

5-25. CAPSTAN SERVO HIGH-SPEED FORWARD ADJUSTMENT. The high-speed forward adjustment principles and requirements are the same as the forward and reverse drive adjustment. Ensure that all previous adjustments are within tolerance.

a. Load the test tape on the transport and connect a counter to the appropriate channel preamplifier output.

b. On the capstan servo PCA place unit in high-speed forward mode with the high-speed forward (+160) service switch (figure 5-3), and use the high-speed forward (+160) adjustment (R53) to adjust speed until counter indicates 53,333 ± 1000 Hz. If adjustment is required, adjust until the counter indicates between 53,233 and 53,433.

c. If unit requires high speed other than 160 ips, the frequency indication of the counter should be (333.3) x (speed).

5-26. CAPSTAN SERVO HIGH-SPEED REVERSE ADJUSTMENT. The high-speed reverse adjustment is identical the the high-speed forward adjustment, except that the control switch (front of tape drive) REWIND pushbutton is used to place the unit in the high-speed reverse mode and the high-speed reverse (-160) variable resistor (R60) is used.

5-27. ALTERNATE METHOD FOR CAPSTAN SERVO ADJUSTMENT.

NOTE: This method is to be used only if a transport test tape and a frequency counter are not available. This method further increases the tolerance and should be used ONLY when proper equipment is not available and the situation is critical.

a. Equipment needed, master skew tape (9162-0027) and Oscilloscope HP model 180 or equivalent.

b. Calculate the data clock period using the following formula:

$$\text{Period} = \frac{1}{\text{Density} \times \text{Speed}}$$

5-34. FORWARD STATIC SKEW COMPENSATION ADJUSTMENTS. The techniques for rapid adjustment and for evaluating the need for adjustment differ. Figure 5-8 shows poor skew alignment and proper skew alignment. (Three possible waveforms due to configurations.) To adjust static skew compensation proceed as follows:

a. Load the Master Alignment Tape, HP part number 9162-0027, and place the tape unit in synchronous forward mode for the adjustment operation.

b. Adjust FWD skew delay control of channel 2 (Read data PCA) until resistor is approximately ¼ turn from the fully CCW position. Channel 2 will be reference channel for the remaining adjustments.

c. Connect the oscilloscope channel A probe to the SKEW test point of the reference channel (2). Connect the oscilloscope channel B probe to each SKEW test point in succession and algebraically add oscilloscope channels A and B.

d. Adjust the oscilloscope sweep to display at least one full bit time (leading edge of one bit to the leading edge of the next), with the oscilloscope vertical deflection at approximately 2V/cm.

e. Adjust each channel skew delay variable resistor for a maximum displayed amplitude (trailing edge in vertical alignment) per waveforms shown in figure 5-8.

5-35. REVERSE STATIC SKEW COMPENSATION ADJUSTMENTS. Reverse static skew compensation is accomplished in exactly the same manner as that used for forward skew except for the use of reverse drive mode and adjustment of reverse skew controls. The same SKEW test points are used for both adjustments.

5-36. READ CHARACTER GATE ADJUSTMENTS. The read character gate is adjusted to allow a period equal to approximately 46 percent of the bit-to-bit distance for all of the read bits in a character to be placed in the output register.

a. Load the tape unit with the Master Alignment Tape, HP part number 9161-0027 (or any all "ones" 800 cpi tape), place the unit in synchronous forward operation, and select 800 cpi operation (multiple density units only).

b. Synchronize the oscilloscope (negative slope) to the NOR test point on the read control card. (The first data bit of a character will start the gate time when this line goes to ground).

c. Observe the bit-to-bit time (negative-going edge to negative-going edge). The low (or ground) portion of this signal represents the character gate time.

d. Using the gate control (R29) on the read control PCA, adjust the NOR (ground portion) of the signal to 46 percent of the nominal bit-to-bit time. Ensure that the bit-to-bit time is consistent with the data transfer rate (i.e. 50 micro-seconds for a 7970 operating at 25 IPS - 800CPI).

NOTE: Figure 5-9 can be used as a guide once the reader is familiar with the forgoing procedures.

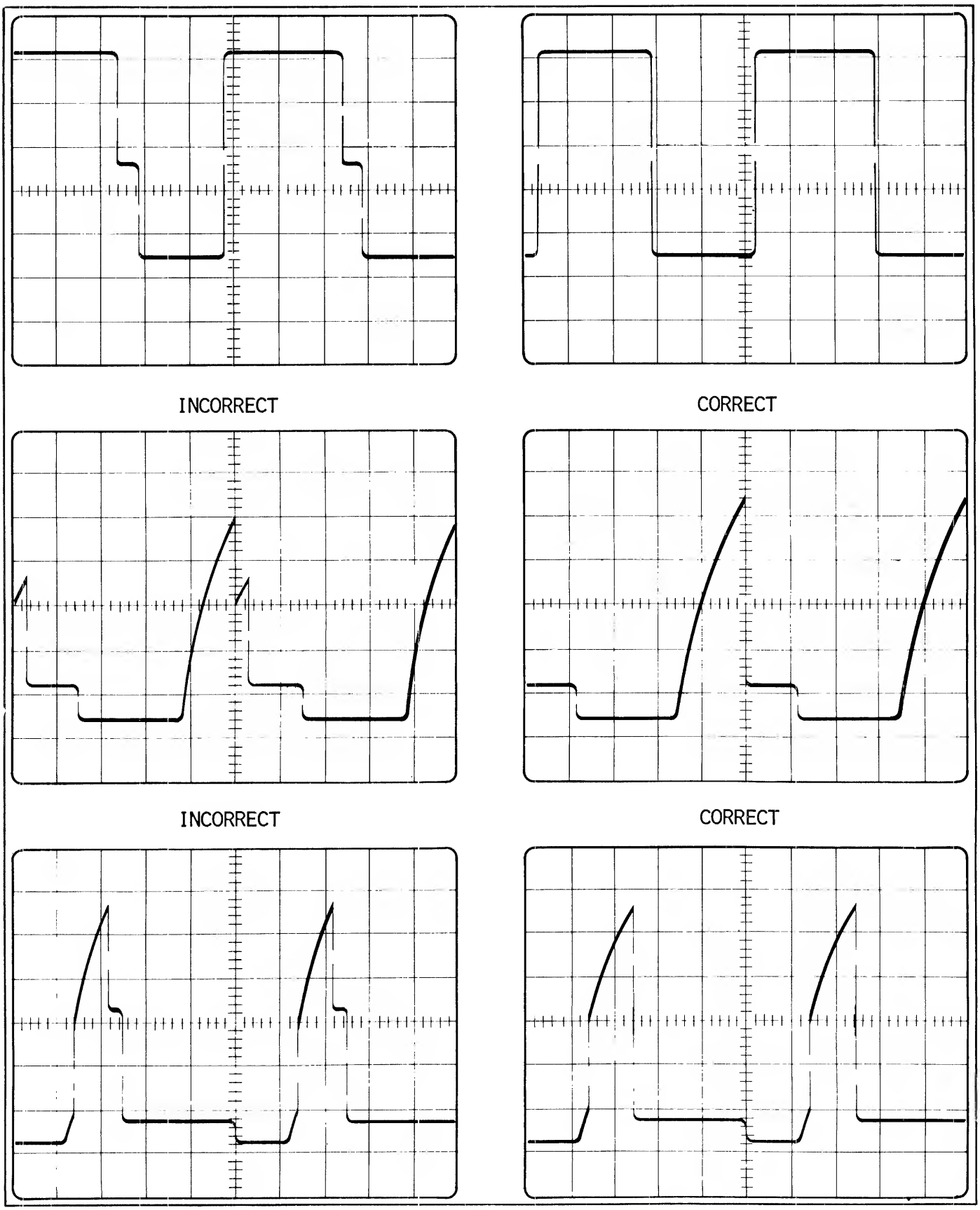


Figure 5-8. Skew Waveforms

h. Bring the tape to the beginning of part A, section 3.

i. Short the LWRITE test point on the data and status PCA to ground and set the tape into forward motion. The MTE, and EOB indicators on the read data test PCA should light. The EVEN, RC, and STE indicators should remain off.

5-61. CLOCK SYNCHRONIZATION PERFORMANCE TEST. This test checks the clock and clock control logic synchronization function while reading a section of tape with a short-term density variation of ±15 percent. Step d checks the ability of the clock to keep synchronized to the incoming data. Steps e and f check that the clock control logic will synchronize the clock to the parity channel Sync Pulse when the channel two Sync Pulse is disabled. Step g checks that the clock control logic causes the clock to operate at its fixed frequency in read-after-write mode.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install PE data test tape, part number 5080-4555, in the tape unit.

c. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

d. Bring the tape to the beginning of section 4. Set tape into forward motion and read the tape for at least 30 seconds. The RC and EOB indicators on the read data test PCA should light and the STE and MTE indicators should remain off.

e. Bring the tape to the beginning of section 4 and short the DIFF test point on the channel two preamplifier to ground.

f. Set the tape into forward motion and read the tape for at least 30 seconds. The STE indicator on the read data test PCA should light and the MTE indicator should remain off.

g. Remove the short from the channel two DIFF test point and short the LWRITE test point on the data and status PCA to ground. Set the tape into forward motion. The MTE indicator should alternate between an on and off condition. STE and EVEN may randomly blink on and off.

5-62. STATUS LOGIC PERFORMANCE TEST. This test checks the portion of the status logic which controls the $\overline{SD16}$ and the MREV signals. The other signals generated by the status logic are checked by other performance tests. Steps d through h check the logic which generates the $\overline{SD16}$ signal. Step i checks the MREV signal as initiated by the $\overline{REV}$ 1 signal from a slave unit.

a. On tape units with a density select switch on the front panel, select 1600.

b. Install the following PCA's in the tape unit under test:

(1) Control and status test PCA, part number 13191-60010.

(2) Read data test PCA, part number 13196-60000.

c. Install a scratch tape in the tape unit.

d. With the tape unit selected and on line (a high present at TP3 on control and status PCA) and the tape stopped, check that the SD16 indicator on the read data test PCA is on.

e. Disconnect the unit select jumper on control and status test PCA (13191-60010). This de-selects the tape unit. Then reconnect the jumper; the SD16 indicator should be off while the jumper is disconnected.

f. If the tape unit has an 800 density switch, select 800 density; then select 1600 density. The SD16 indicator should be off while 800 density is selected.

g. Place the tape unit off line by pressing the RESET pushbutton on the tape unit front panel. The SD16 indicator should be off.

h. With the tape unit still off line, short pins 24 and 24X together at connector J16 on the master PE read motherboard. The SD16 indicator should be on while the two pins are shorted together.

i. Set the tape into forward motion and short pins 23 and 23X at slave connector J16 on the PE master motherboard. The MTE indicator on the read data test PCA should light while the short is in place.

5-63. PE READ PREAMPLIFIER GAIN PERFORMANCE TEST (READ-ONLY UNITS). Before performing the following procedures, ensure that the tape transport long-term speed variation is within specification. To check the preamplifier gain, proceed as follows:

a. Install reference amplitude test tape, part number 5080-4548, in tape unit.

b. If the tape unit under test has 1600 density select switch front panel, select 1600.

c. Connect oscilloscope probe to DIFF test point on read preamplifier PCA for parity channel (PE test point on seven/nine-track tape units).

d. Set tape into forward motion at synchronous speed using CF switch on control and status PCA. Observe waveform, average peak-to-peak amplitude should be 4.0 $\pm$ 0.1 volts.

NOTE: Due to age and handling, a reference tape does not have the degree of magnetism that was originally written, thus gains set up to this standard will be set high. If this is suspected, the gains can be checked with recently written data tapes; the gain should be set as close to 4.1 VPP as possible.

e. Repeat steps c and d for each of the remaining channels (zero through seven).

5-64. PE READ PREAMPLIFIER GAIN PERFORMANCE TEST (READ/WRITE UNITS). Before performing the following procedures, ensure that the tape transport long-term speed variation is within specification. To check the preamplifier gain of read/write units, proceed as follows:

a. Install a scratch certified 3200 frpi tape in tape unit.

b. Install control and status test PCA, part number 13191-60010, PE write formatter, part number 13195-60000, and write formatter test PCA, part number 13196-60001 in the tape unit.

c. Connect oscilloscope probe to DIFF test point of read preamplifier for the parity channel and set up the test PCA's listed in step b as follows:

Write formatter test PCA. Test plug in position corresponding to tape drive speed.

PE Write Formatter. Data Select-1600 frpi Data Block-ON.

Control and Status WSW-ON (up) CF-ON (up).

d. The tape unit is now writing continuous 1600 frpi in all nine channels. Measure average peak-to-peak amplitude of signal as shown in the oscilloscope at DIFF test point. The oscilloscope should read 4.5 $\pm$ 0.1 Vpp. Adjust gain potentiometer, if necessary, to this specifications.

NOTE: A feed-through signal (crosstalk) from the write head can cause minor distortion on the DIFF test point signal. The limits indicated in step d refer to portions of the test point signal which are free of obvious write head feed-through distortion.

e. Adjust oscilloscope to display several cycles of DIFF test point signal. Waveforms should be free of clipping and discontinuities (ignore slight distortion caused by crosstalk).

f. Repeat steps c through e for each of the eight remaining channels.

5-65. PE THRESHOLD LEVEL PERFORMANCE TEST (READ-ONLY UNITS). To check the threshold level of a PE master read-only tape unit, proceed as follows:

a. Install a scratch tape in the tape unit.

b. Connect the common (ground) lead of a dc voltmeter, with an accuracy of one percent or better, to the GND test point on the PE data and status PCA (master units) or the GND test point on the PE slave read PCA (slave units).

c. Set tape unit into forward tape motion and use voltmeter to check voltage at +THR and -THR test points on PE data and status PCA. They should be as follows:

+THR: +0.30 ± 0.02 Vdc.
-THR: -0.30 ± 0.02 Vdc.*

* -THR used on 07970-62041 PCA only

5-66. PE THRESHOLD LEVEL PERFORMANCE TEST (READ/WRITE UNITS). To check the threshold level of a PE read/write tape unit, proceed as follows:

a. Install a scratch tape in the tape unit.

b. Connect the common (ground) lead of a dc voltmeter, with an accuracy of one percent or better, to the GND test point on the PE data and status PCA (master units) or the GND test point on the PE slave read PCA (slave units).

c. Connect a source of +5 Vdc to TP1 (WSW signal) of the control and status PCA.

d. Set tape unit into forward tape motion and use voltmeter to check voltage at +THR and -THR test points on PE data and status PCA. They should be as follows:

+THR: +0.77 ± 0.02 Vdc.
-THR: -0.77 ± 0.02 Vdc.*

* -THR used on 07970-62041 PCA only

5-67. STATIC SKEW PERFORMANCE TEST. Before performing the following test, ensure that the tape transport is operating properly. To check the static skew, proceed as follows:

a. Install master alignment tape, part number 9162-0027, in tape unit.

NOTE: Waveforms for a slave unit can be monitored at the DAT test points on the read decoder PCA's in the master unit, provided the slave unit is connected to the master unit and selected on the master unit select switch. If the slave unit is not connected to the master unit, monitor the waveforms at the test points on connector P2 of the slave read PCA. The test point for master units is the DAT test point on the read decoder PCA.

b. Connect oscilloscope channel A probe to test point for parity channel.

c. Connect oscilloscope channel B probe to DAT test point on read decoder PCA for channel two. (Channel two is used as the reference channel).

d. Set tape unit for synchronous speed forward and adjust oscilloscope sweep to trigger on positive edge of whichever waveform goes positive first. (If parity channel waveform goes positive before channel two waveform, trigger oscilloscope sweep on parity channel waveform; otherwise trigger oscilloscope sweep on channel two waveform).

The HP 13191A Control and Status Test Board Accessory is available for use with the tape unit. With this test board it is possible to completely adjust and verify the performance of the control and status function of a tape unit under off-line conditions. Complete details covering this item is included with the accessory. The HP 13191A Control and Status Test Board Accessory provides a normal drive modes as well as cyclic programming which is suitable for adjustment of the capstan start-stop ramp. The test board also includes status indicator lamps to verify all normal status functions. The test board is installed in the connector of the tape unit control and status PCA.

5-82. TEST EQUIPMENT REQUIRED. Test equipment required for performance testing of the tape transport is as follows:

a. Control and status test PCA, part number 13191-60010.

b. Oscilloscope, HP 180, dual trace or equivalent.

c. Multimeter/counter 5000A or equivalent.

d. Master alignment tape, part number 9162-0027.

e. Transport speed test tape, part number 5081-9401.

5-83. CAPSTAN MOTOR OFFSET CURRENT. Connect a suitabe dc voltmeter or oscilloscope across the 1.5 ohm, 1 percent resistance (comprised of R21 and R22 in parallel). The common sides of the resistors are connected to pin 2 of CJ-1. With the tape under tension but not tape motion, the voltage should not exceed the following (reference to 0 Vdc).

a. Maximum acceptable operating limit: $\pm$100 mV dc at 25°C.

b. Adjustment recommended if greater than: $\pm$80 mV dc. (Refer to alignment section).

5-84. LONG-TERM SPEED VARIATION. The long-term tape speed variation is measured by using a frequency counter to count the signals at the output of one of the read preamplifiers while reading a tape with highly accurate between-character spacing. The signal frequency at the preamplifier output is used as a measure of tape travel per second, HP transport speed test tape, part number 5081-9401, provides a between-character spacing accuracy better than 0.1 percent. Reference frequencies listed below are based on use of this tape. To check long-term speed variation, proceed as follows:

a. Connect a frequency counter to the output of the channel three preamplifier.

b. Install transport speed test tape, part number 5081-9401.

c. Use the three switches on the capstan servo printed-circuit assembly and the REWIND switch on the front panel to control tape motion while checking the tape

speeds listed below.

NOTE: To derive tape speed frequencies not supplied, use the following equation:

FREQUENCY (in Hz) = 333.33 X TAPE SPEED (in ips)

(1) Forward and Reverse Drive: Frequency depends on tape speed and must be calculated for speeds other than 25 ips, 37.5 ips and 45 ips which are listed below. Maximum acceptable operating limit is based on ±1 percent with adjustment recommended if speed error is +0.8 percent or greater.

a. The 25 ips drive nominal frequency is 8,333 Hz. Acceptable limits are ±83 Hz.

b. The 37.5 ips drive nominal frequency is 12,500 Hz. Acceptable limits are ±125 Hz.

c. The 45 ips drive nominal frequency is 15,000 Hz. Acceptable limits are ± 150 Hz.

(2) Loadpoint Search: 20 ips; basic frequency is 6,667 Hz.

a. Maximum acceptable limit is ±1,330 Hz (±20 percent).

b. No adjustment is provided.

NOTE: The half-speed forward and half-speed reverse checks, as listed below, are applicable only to tape units with a dual-speed capstan servo printed-circuit assembly.

(3) Half-Speed Forward and Half-Speed Reverse: 22.5 ips, basic frequency is 7,500 Hz.

a. Maximum acceptable limits are ±75 Hz (±1 percent).

b. Adjustment recommended if greater than ±60 Hz (±0.8 percent).

(4) High-Speed Forward: 160 ips, basic frequency is 53,333 Hz.

a. Maximum acceptable operating limit: ± 1000 Hz (±2 percent).

b. Adjustment recommended if greater than: ±800 Hz (±1.5 percent).

(5) Rewind (High-Speed Reverse): Checked identically to the limits applicable to high-speed forward, except that the rewind mode is used.

5-85. TENSION ARM POSITION. With no tape motion, the tension arms should be aligned with the centering marks on the rear of the casting. Adjustment is required if the arm is out of position by more than the diameter of the arm.

5-119. PE READ PREAMPLIFIER GAIN PERFORMANCE TEST (READ-ONLY UNITS). Before performing the following procedures, ensure that the tape transport long-term speed variation is within specification. To check the preamplifier gain, proceed as follows:

a. Install reference amplitude test tape, part number 5080-4548, in tape unit.

b. If the tape unit under test has 1600 density select switch on front panel, select 1600.

c. Connect oscilloscope probe to DIFF test point on the read preamplifier PCA for the parity channel (PE test point on seven/nine-track tape units).

d. Set tape into forward motion at synchronous speed and observe waveform. Average peak-to-peak amplitude should be 4.0 $\pm$ 0.1 volts.

e. Repeat steps c and d for each of the remaining channels (zero through seven).

5-120. PE READ PREAMPLIFIER GAIN PERFORMANCE TEST (READ/WRITE UNITS). Before performing the following procedures, ensure that the tape transport long-term speed variation is within specification. To check the preamplifier gain of read/write units, proceed as follows:

a. Install a scratch certified 3200 frpi tape in tape unit.

b. Install control and status test PCA, part number 13191-60010, PE write formatter, part number 13195-60000, and write formatter test PCA, part number 13195-60001 in the tape unit.

c. Connect oscilloscope probe to DIFF test point of read preamplifier for parity channel.

NOTE: A feed-through signal from the write head will be observed riding on the test point signal. The limits indicated in the following step refer to portions of the test point signal which are free of obvious write head feed-through distortion.

d. Use test PCA's listed in step b to write continuous 1600 frpi in all nine tape channels. While writing, measure average peak-to-peak amplitude of the pre-amplifier signal at test point. Peak-to-peak amplitude should be 4.5 $\pm$ 0.1 volts.

e. Adjust oscilloscope to display several cycles of test point signal. Waveforms should be free of clipping and discontinuities (ignore write head feed-through signals).

f. Repeat steps c through e for each of the eight remaining channels.

5-121. PE THRESHOLD LEVEL PERFORMANCE TEST (READ-ONLY UNITS). To check the threshold level of a PE master read-only tape unit, proceed as follows:

a. Install a scratch tape in the tape unit.

b. Connect the common (ground) lead of a dc voltmeter, with an accuracy of one percent or better, to the GND test point on the PE data and status PCA (master units) on the GND test point on the PE slave read PCA (slave units).

c. Set tape unit into forward tape motion and use voltmeter to check voltage at +THR and -THR test points on PE data and status PCA. They should be as follows:

+THR: +0.30±0.02 Vdc.
-THR: -0.30±0.02 Vdc. (-THR used on 07970-62041 PCA only)

5-122. PE THRESHOLD LEVEL PERFORMANCE TEST (READ/WRITE UNITS). To check the threshold level of a PE read/write tape unit, proceed as follows:

a. Install a scratch tape in the tape unit.

b. Connect the common (ground) lead of a dc voltmeter, with an accuracy of one percent or better, to the GND test point on the PE data and status PCA (master units) or the GND test point on the PE slave read PCA (slave units).

c. Connect TP1 (WSW signal) of the control and status PCA to GND.

d. Set tape unit into forward tape motion and use voltmeter to check voltage at +THR and -THR test points on PE data and status PCA. They should be as follows:

+THR: +0.77±0.02 Vdc.
-THR: -0.77±0.02 Vdc. (-THR used on 07970-62041 PCA only)

5-123. STATIC SKEW PERFORMANCE TEST. Before performing the following test, ensure that the tape transport is operating properly. To check the static skew, proceed as follows:

a. Install master alignment tape, part number 9162-0027, in tape unit.

NOTE: Waveforms for a slave unit can be monitored at the DAT test points on the read decoder PCA's in the master unit, provided the slave unit is connected to the master unit and selected on the master unit select switch. If the slave unit is not connected to the master unit, monitor the waveforms at the test points on connector P2 of the slave read PCA. The test point for master units is the DAT test point on the read decoder PCA.

b. Connect oscilloscope channel A probe to DAT test point on read decoder PCA for the parity channel.

c. Connect oscilloscope channel B probe to DAT test point on the read decoder PCA for channel two. (Channel two is used as the reference channel).

d. Set tape unit for synchronous speed forward and adjust oscilloscope sweep to trigger on positive edge of whichever waveform goes positive first. (If parity channel waveform goes positive before channel two waveform, trigger oscilloscope sweep on parity channel waveform; otherwise trigger oscilloscope sweep on channel two waveform).

e. Adjust oscilloscope for alternate display of channels A and B.

f. Estimate and record average time difference between positive edges of waveforms. Also, record whether parity channel waveform occurs before or after channel two waveform.

g. Repeat steps b and d through f for channels zero, one, and three through seven. Leave oscilloscope channel B connected to channel two (reference channel).

h. Add largest time difference by which a waveform precedes channel two waveform plus largest time difference by which a waveform follows channel two waveform.

i. Multiply sum of largest leading and lagging time differences (in microseconds) by tape speed (in inches/second) to obtain static skew in microinches. Skew should be less than 300 microinches.

5-124. PHASE ENCODED WRITE CIRCUITS PERFORMANCE TESTS.

Performance tests on the PE write circuits consist of an overall performance test and tests for uncompensated write skew, erase phasing, assymmetry of write time for each data bit, crosstalk from the write heads to the read heads, and efficiency of the erase heads.

5-125. TEST EQUIPMENT. Test equipment required to check performance of the PE write circuits is as follows:

a. Control and status test PCA, part number 13191-60010.

b. Read data test PCA, part number 13196-60000.

c. Write formatter PCA, part number 13195-60000.

d. Write formatter test PCA, part number 13196-60001.

e. Oscilloscope, HP 180A dual trace, or equivalent.

f. Scratch certified 3200 frpi tape.

5-126. OVERALL WRITE PERFORMANCE TEST. The following test is useful for checking the write capability of the write circuits. However, since the master PE read circuits are used as test equipment in this test, it is necessary that they be operating correctly.

NOTE: If the tape unit under test is a slave unit, it will be necessary to connect it to the master unit to perform this test.

a. Install the following test PCA's in the master tape unit:

(1) Control and status test PCA, part number 13191-60010.

(2) Write formatter PCA, part number 13195-60000.

(3) Write formatter test PCA, part number 13196-60001.

b. Install the read data test PCA, part number 13196-60000 in the unit under test.

c. Install a scratch tape in the tape unit under test and bring it to the load point.

d. On the write formatter test PCA, set the switches as follows:

SWITCH	POSITION
DATA SELECT	SINGLE ROTATING BIT
END OF DATA	Right position
DATA BLOCKS	Left position
WRITE ID BURST	Left position
TAPE MARK	Left position
Thumb Wheel Variable Resistor	fully counterclockwise

e. On the write formatter PCA, make sure the speed jumper is set to the speed of the unit under test and the jumper near chip U32 is from 2 to 3.

f. On the control and status test PCA, select WSW.

g. Press the ON LINE switch on the tape unit front panel, then set the tape into forward moton using the CF switch on the control and status test PCA. The SD16 indicator on the read data test PCA should be on and the RC and EOB indicators should be off.

h. Set the DATA BLOCKS switch on the write formatter test PCA to the right position. The RC and EOB indicators should flash, the EVEN, STE, and MTE indicators should remain off, the 7 channel should be on bright, and the remaining channel indicators should be on dim.

5-127. UNCOMPENSATED WRITE SKEW PERFORMANCE TEST. This test measures the amount of write skew before it is adjusted out using the skew adjustment variable resistors on the write data PCA's.

NOTE: When running a particular section of the tape, use care not to over-run into the next tape section. To do so would produce misleading indications.

Action of the indicators on the read data test PCA (such as the EOB, IDB, and TM indicators) is dependent on tape speed. At low tape speeds, the indicators which light at a certain point in the tape block will flicker when a succession of blocks are read. At high speeds, the same indicators might stay on steadily. This occurs because, at high speeds, the off time of the input signal is not sufficient to turn off the indicator.

As an added tool for further troubleshooting, refer to the available diagnostic tests.

It is possible that some problems in the Photosense Assembly (HP P/N 07970-61150 or 07970-62131) can cause the tape unit BOT (Beginning-of-tape) and EOT (End-of-tape) logic circuits to malfunction.

If failure occurs, as described above, determine the following:

a. Photosense assembly is positioned correctly.

b. The proper maintenance (paragraph 5-11) has been performed on schedule.

c. If by tapping in the area of the photosense PCA, the light will go brighter and dimmer, the lamp is not seated tightly in its base; retension the retaining tab.

d. With the tape positioned such that the BOT tab is <u>not</u> under the Photosense Head, the output voltage should be -.4 Vdc or greater (more negative). If the voltage is less than -.4 Volts, try repositioning the Photosense Head Assembly closer to the tape but remaining parallel to the tape.

NOTE: The normal position of the Photosense Head is such that the face of the assembly is parallel to the path of the tape and approximately 1/8 inch from the tape. Try to maintain parallelism and position the head no closer than 1/16 inch from tape path.

e. Position the BOT tab under the Photosense Head, the output voltage should be + 1.2 Vdc or greater. If less than + 1.2 volts, try repositioning the Photosense Head Assembly relative to the tape. See note above.

5-158. BOT, EOT DETECTION PROBLEMS

If none of the above solve the problem, replace the Photosense Assembly. In the event that modular repair is not possible, the following can be used to select the proper biasing Resistors for Q1 and Q2.

NOTE: THE AVERAGE BIASING RESISTOR IS 2 MEG-OHM.

a. Install an IBM master alignment tape (9162-0027) on the 7970.

b. Connect an Oscilloscope to the output of the BOT (J3 Pin 8) or BOT test point on the Control Switch Assembly.

c. With the tape positioned such that the BOT tab is not under the Photosense Head, the output voltage should be -.4Vdc or greater. (more negative). If the voltage is less than -.4 volts, decrease the value of resistor R2.

d. Position the BOT tab under the Photosense Head, the output voltage should be + 1.2 volts or greater. If less than + 1.2 volts, increase the value of resistor R2.

e. Repeat steps c and d until the output of the BOT meets the above mentioned outputs. It may be necessary to re-position the Photosense Assembly to obtain results.

NOTE: The normal position of the Photosense Head is such that the face of the assembly is parallel to the path of the tape and approximately 1/8 inch from the tape. Try to maintain parallelism and position the head no closer than 1/16 inch from tape path.

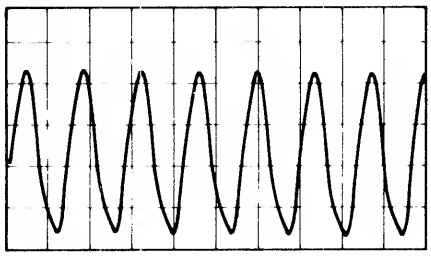
f. Connect the Oscilloscope to the output of the EOT, (J3 Pin 9) or the EOT test point on the Control Switch Assembly.

g. Repeat steps c, d, and e. If voltage does not meet the output parameters change the value of R4, EOT biasing Resistor, according to the indication observed in steps c and d.

h. Re-check both BOT and EOT to ensure that the output remains within the parameters mentioned in steps c and d.

IDB WAVEFORMS

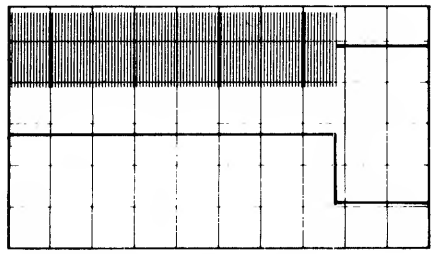
WAVEFORM 1



PE only units
Preamplifier DIFF TP
Dual and multiformat units:
Preamplifier PE TP

Horiz = 20 µs/cm
Vert = 1.0 V/cm

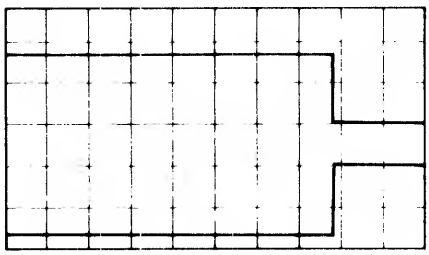
WAVEFORM 2



TRACE A = Parity channel preamplifier DIFF TP (PE only units) or PE TP (dual and multiformat units)
TRACE B = Parity channel decoder PCA LVL TP

Horiz = 10 ms/cm
Vert = 2 V/cm

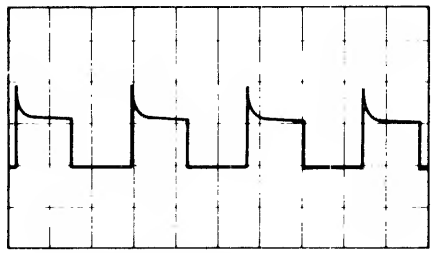
WAVEFORM 3



TRACE A = Parity channel decoder PCA LVL TP
TRACE B = Data and status PCA LIDL TP

Horiz = 10 ms/cm
Vert = 2 V/cm

WAVEFORM 4



Write data PCA HEAD DRIVE TP

Horiz = 10 µs/cm
Vert = 10 V/cm

WAVEFORM 5

Waveform at write interconnect PCA for a typical channel

Horiz = 10 µs/cm
Vert = 5 V/cm

NOTES

1. Normal indications, on the read data test PCA, for IDB blocks are as follows
   a. IDB indicator on for each block
   b. EOB indicator on at end of each block
   c. EOB TP active (low) at end of each block
   d. All other indicators (except SD16) off

7970-543-1

Figure 5-10. Identification Burst Troubleshooting Flowchart (Sheet 1 of 3)

CHANGE 4
DEC, 1977

Manual Part No.: 07970-90887
Print Date: JUN 1976

CHANGE TO:

7970B/E Digital Magnetic Tape Units
Service Manual

CHANGE DESCRIPTION: This change updates the manual to current standards.

CHANGE INSTRUCTIONS:

PAGE 5-22A AND 5-22B

Add paragraph k to section 5-39B and 5-39C following sub-paragraph J.

k. Note the width of the longest positive pulse present at the skew testpoints. It sould be less than 290/V microseconds, where V is the transport speed in inches per second.

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